EK79202

Rev. 0.1

PRELIMINARY DATA SHEET

2052CH Source Driver with TCON MIPI/LVDS Interface

fitipower integrated technology Inc.

Table of Contents

Single Chip 2052 Channel Source Driver With Timing Controller for TFT LCD

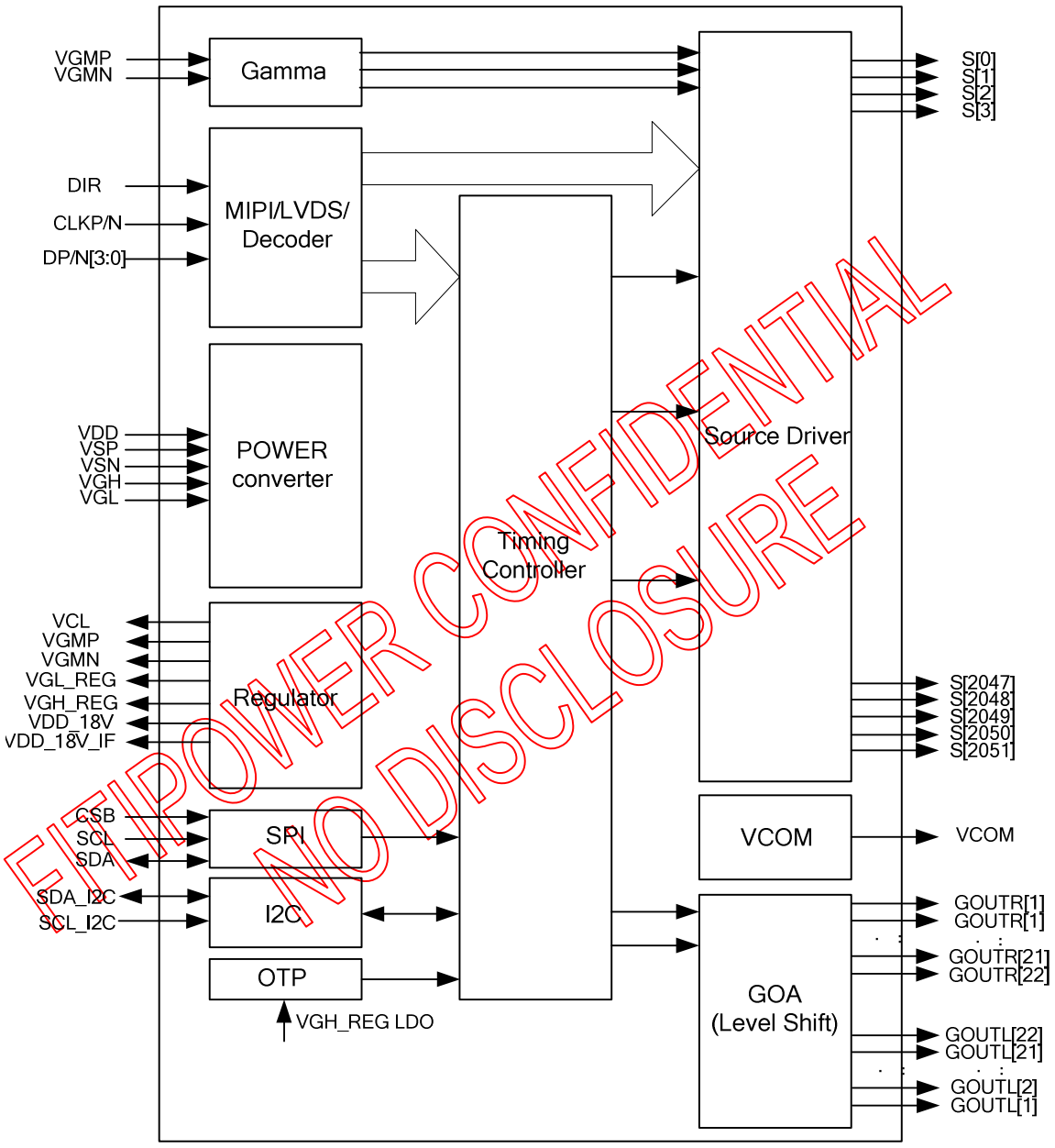
1. General Description

The EK79202 is a highly integrated solution for small size to middle size α-Si TFT-LCD panels. This chip integrates 2052 channel source driver a timing controller for color TFT LCD panel. The chip support MIPI interface and LVDS interface. And support the function setting through R/W SPI/3-wie serial interface

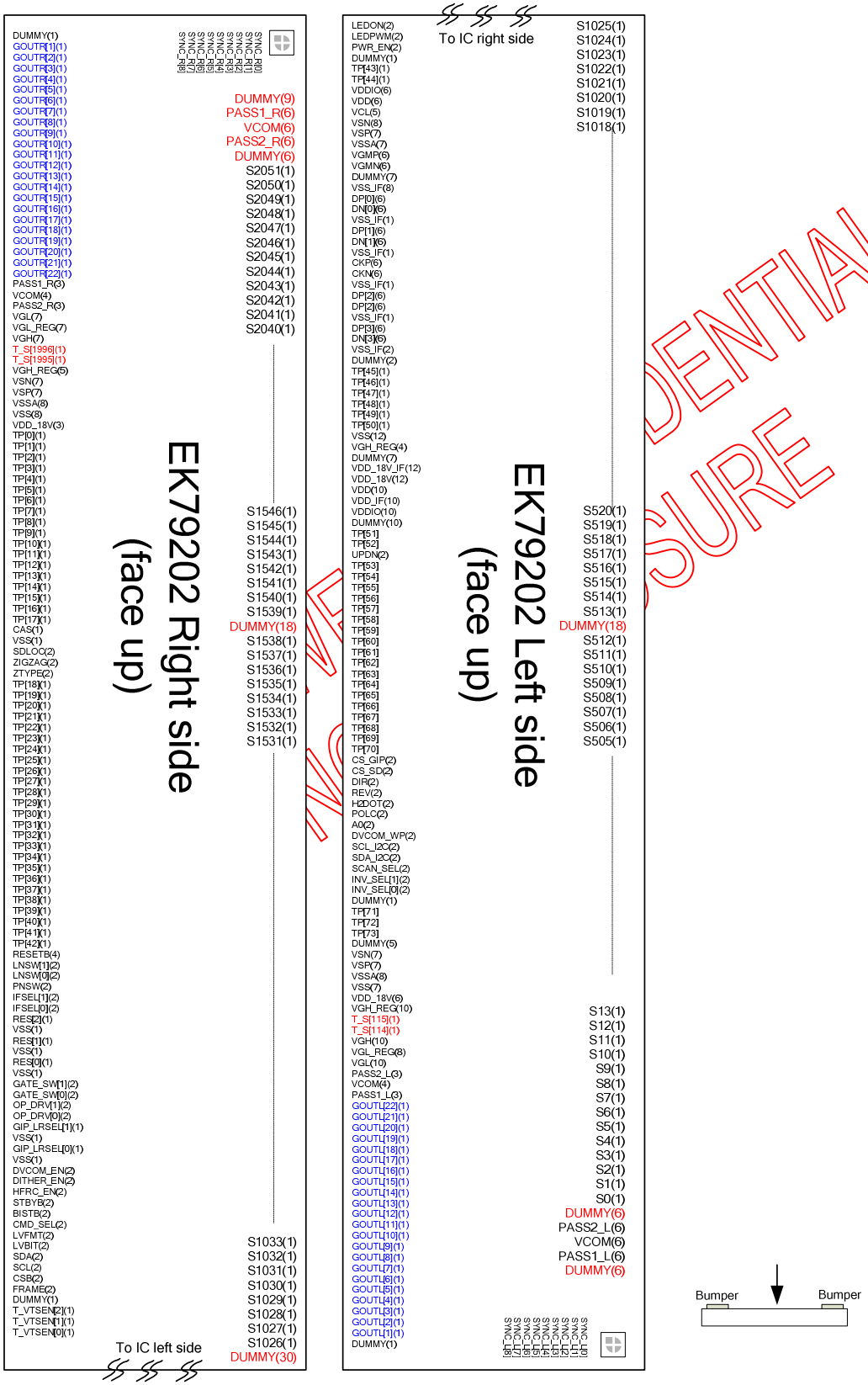
2. Features

- Single chip solution for a WXGA a-Si type LCD display
- Integrate 2052 channel source driver and timing controller
- Display Resolution :
  - 1366 RGB x 768
  - 1280 RGB x 800
  - 1024 RGB x 600
  - 960 RGB x 640
  - 800 RGB x 600
- System Interfaces:
  - MIPI DSI 4Lane / 3Lane
  - LVDS interface (6/8 bit)
- Integrate 2052 channel source driver and timing controller
- Support for Programming Gamma correction
- OTP memory to store initialization register settings
- Support SPI/I2C interface
- Supports Zigzag /Column inversion
- Gate driver control signals for GIP
- Internal level shifter for Gate driver control
- Built-In VCOM generator
- Built-In Enhanced BIST pattern
- Built-In OTP (6Times) to store VCOM calibration
- Built-In OTP (3Times) to store gamma calibration
- COG package
- Input voltage ranges:
  - I/O and interface power supply (VDDIO): 2.3V to 3.6V
  - High speed interface power supply (VDD_IF): 2.3V to 3.6V
  - Power for digital circuit(VDD): 2.3V~3.6V
  - Analog voltage range for VSP: 4.5V to 6.0V
  - Analog voltage range for VSN: -4.5V to -6.0V
  - Analog voltage range for VGH: 11V to 24V
  - Analog voltage range for VGL: -6V to -17V
  - VGH,VGL: VGH-(VGL)<32V
- Output voltage ranges:
  - Analog voltage range for VSP: 4.5V to 6.0V
  - Analog voltage range for VSN: -4.5V to -6.0V
  - Analog voltage range for VCL : -2.8V
  - Positive source output voltage level: VGMP= 3.5V to 5.8V
  - Negative source output voltage level: VGMN= -3.5V to -5.8V
  - Positive gate driver output voltage level: VGH= 11V to 24V
  - Positive gate driver output voltage level: VGH_REG= 9.0V to 22V
  - Negative gate driver output voltage level: VGL = -6V to -17V
  - Negative gate driver output voltage level: VGL_REG= -4.5V to -15V
  - VCOM= -0.5V to -2.405V , step=15mV (7-bit resolution)
  - VGH,VGL: VGH-(VGL)<32V

3. Chip Function Block Diagram



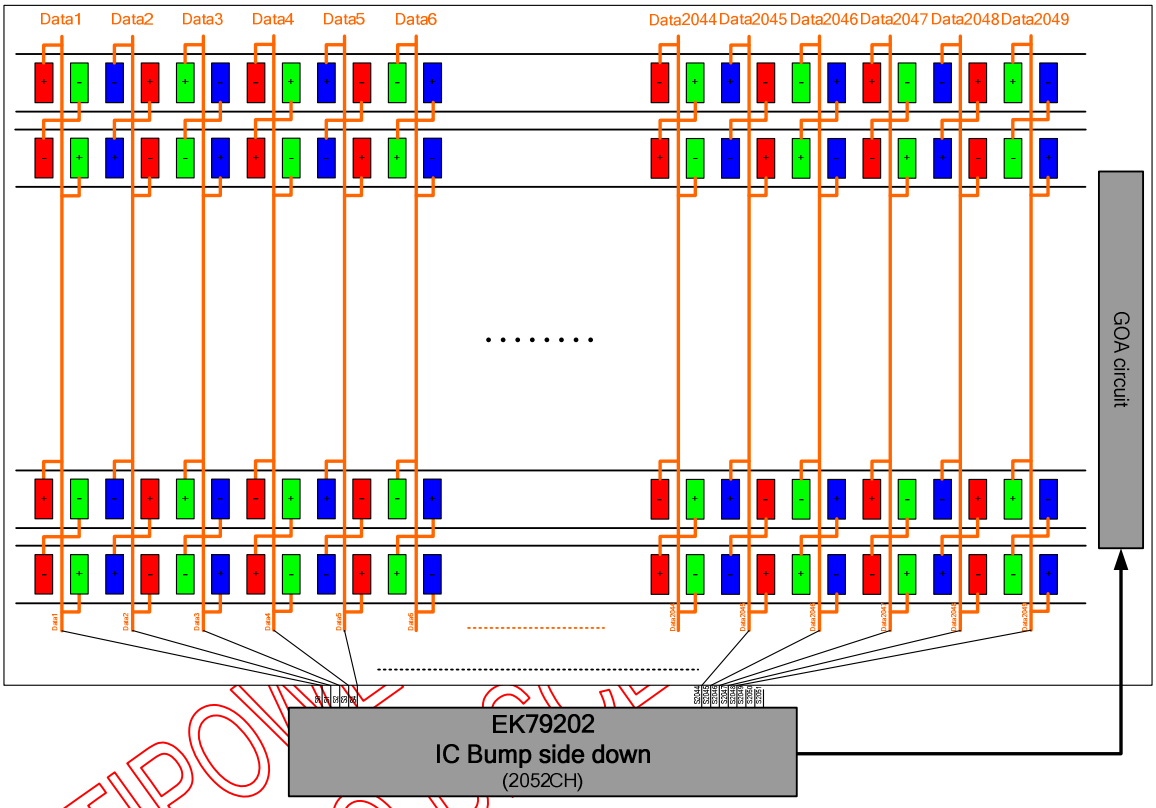
4. Pad Arrangement



5. Application Diagram with Panel

5.1 GIP Application_1366RGBx768 (Normal Dual Gate Driving)

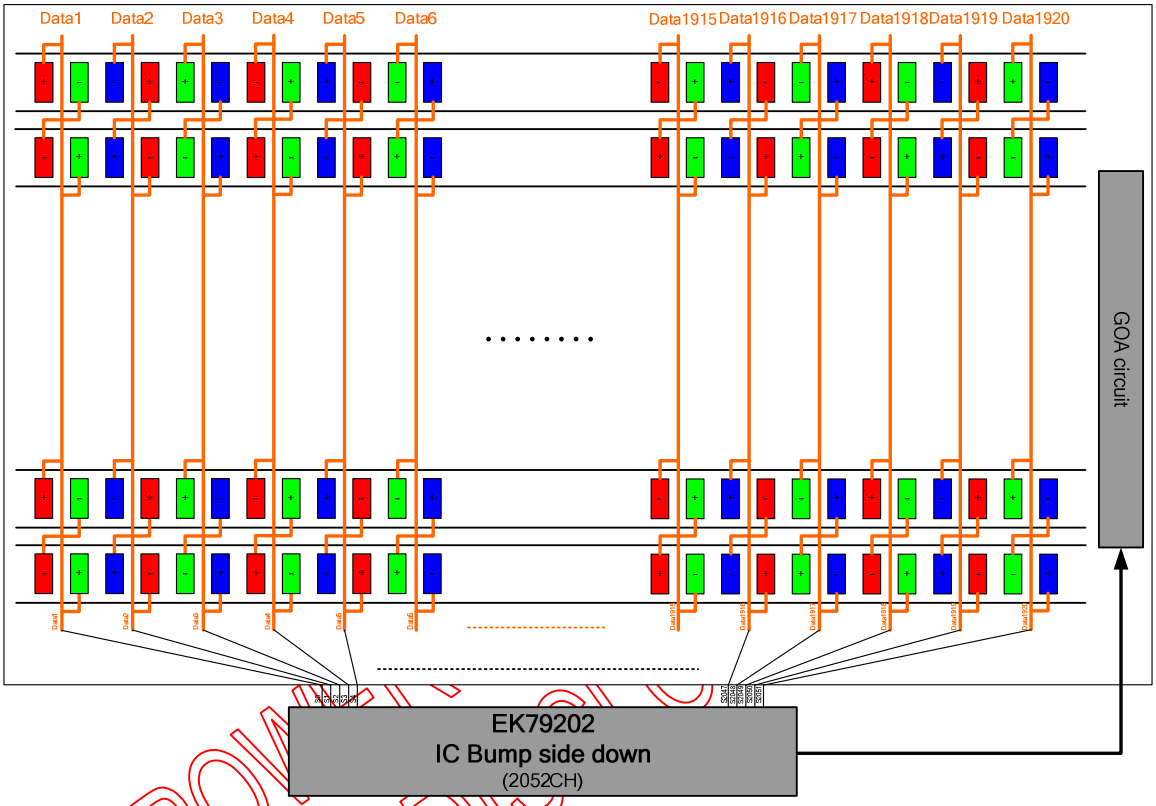
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1366RGBx768	S[2051:0]	-

5.2 GIP Application_1280RGBx800 (Normal Dual Gate Driving)

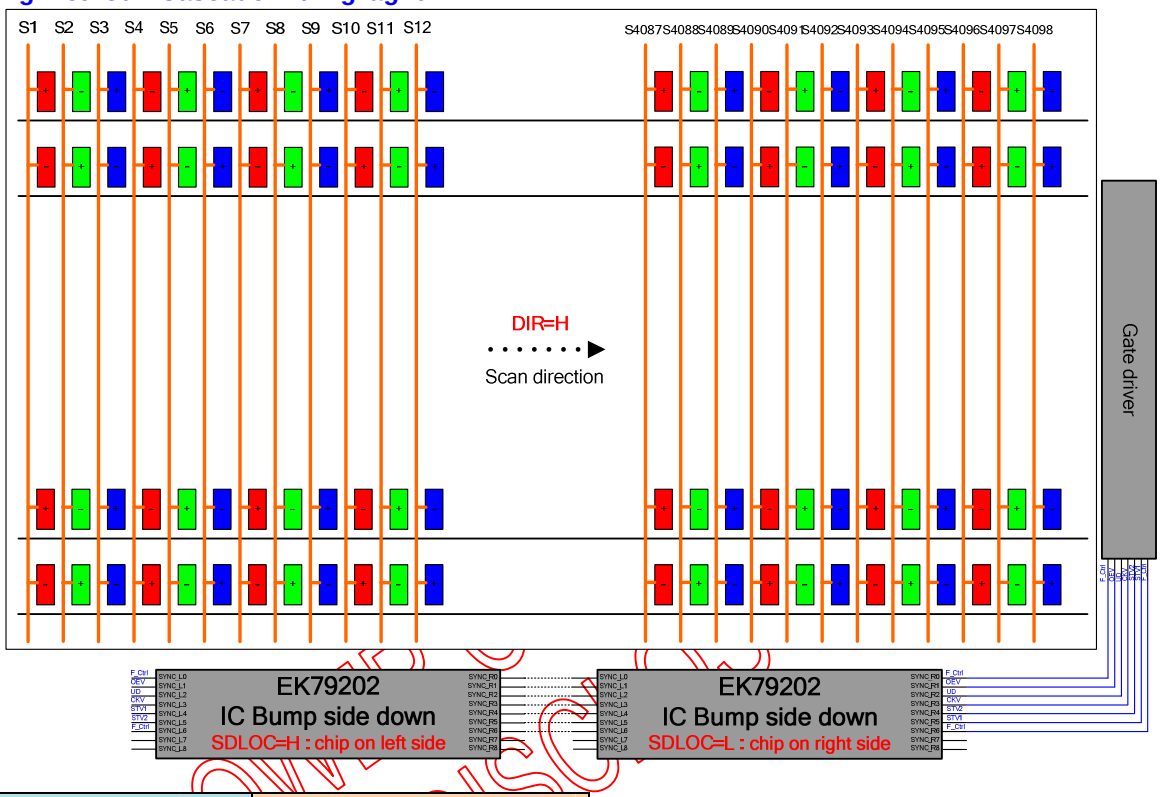
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1280RGBx800	S[959:0] and S[2051:1092]	S[1091:960]

5.3 Cascade Application – Gate driver mode1

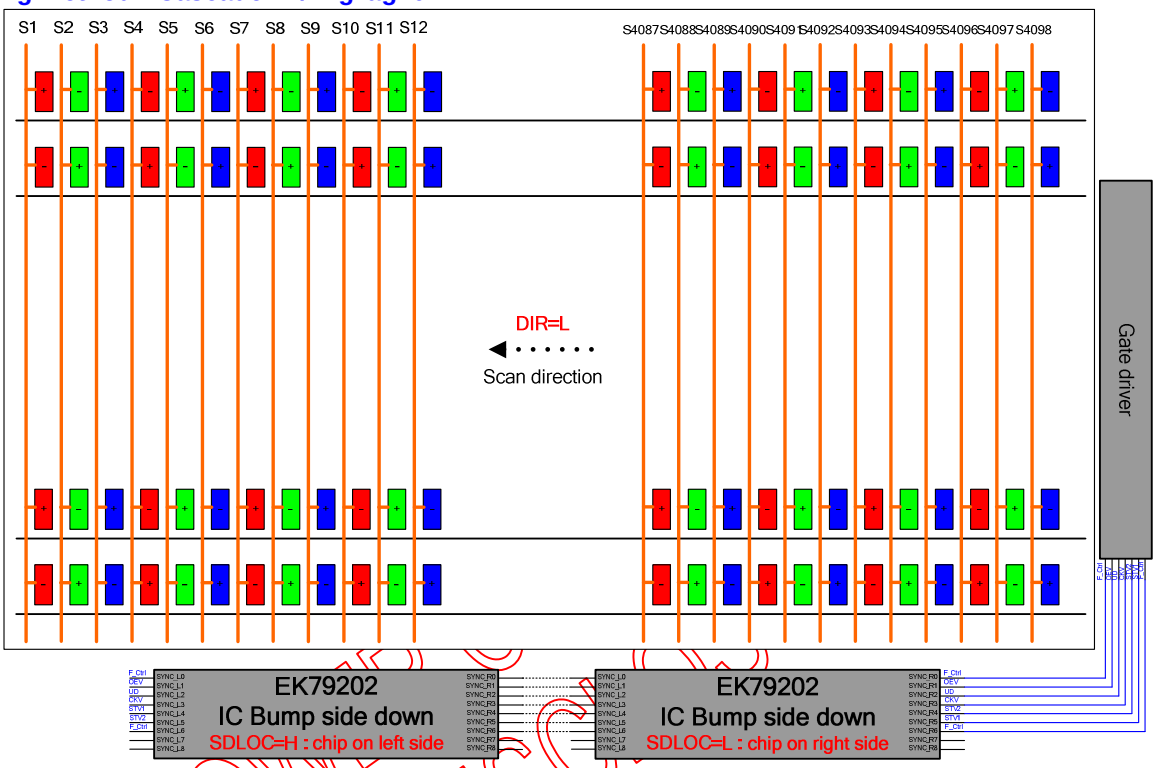
Driving method : Cascade=1 / Zigzag=0



SDLOC=H : chip on left side		SDLOC=L : chip on right side	
Pad name	Output signal	Pad name	Output signal
SYNC_L0	F_Ctrl	SYNC_R0	F_Ctrl
SYNC_L1	OEV	SYNC_R1	OEV
SYNC_L2	UD	SYNC_R2	UD
SYNC_L3	CKV	SYNC_R3	CKV
SYNC_L4	STV1	SYNC_R4	STV2
SYNC_L5	STV2	SYNC_R5	STV1
SYNC_L6	F_Ctrl	SYNC_R6	F_Ctrl
SYNC_L7	-	SYNC_R7	-
SYNC_L8	-	SYNC_R8	-

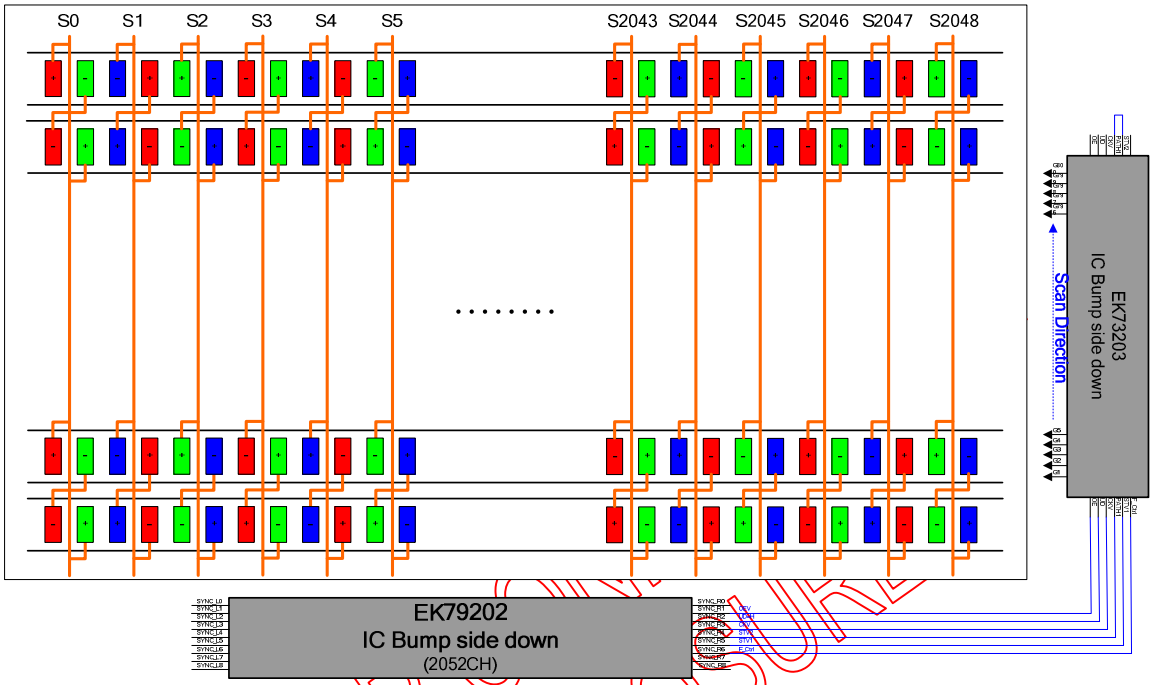
5.4 Cascade Application – Gate driver mode2

Driving method : Cascade=1 / Zigzag=0

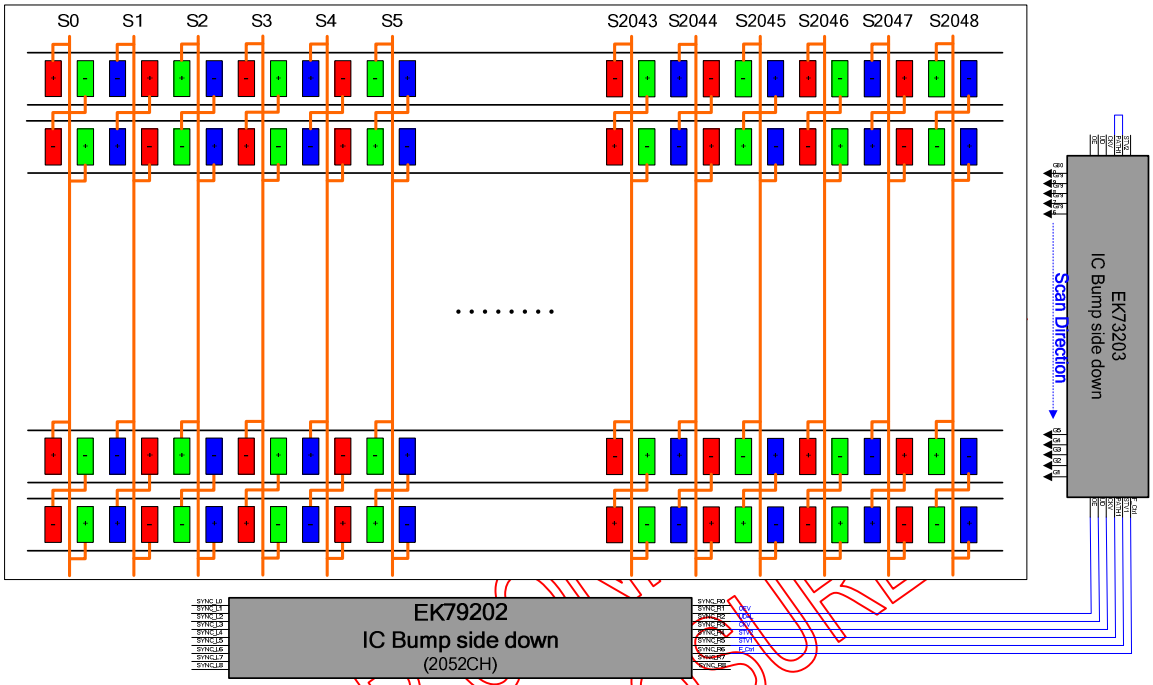


SDLOC=H : chip on left side		SDLOC=L : chip on right side	
Pad name	Output signal	Pad name	Output signal
SYNC_L0	F_Ctrl	SYNC_R0	F_Ctrl
SYNC_L1	OEV	SYNC_R1	OEV
SYNC_L2	UD	SYNC_R2	UD
SYNC_L3	CKV	SYNC_R3	CKV
SYNC_L4	STV1	SYNC_R4	STV2
SYNC_L5	STV2	SYNC_R5	STV1
SYNC_L6	F_Ctrl	SYNC_R6	F_Ctrl
SYNC_L7	-	SYNC_R7	-
SYNC_L8	-	SYNC_R8	-

5.5 Gate Driver Application1 – GATE_SW [1:0]=[0:0]



5.6 Gate Driver Application2 – GATE_SW [1:0]=[0:0]



6. Pin Function Description

6.1 Pin define

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td colspan="3">Interface and Control</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>Input</td><td>MIPI or LVDS data Input.
Select by IFSEL[1:0] pin</td></tr>
<tr><td>CKP/CKN</td><td>Input</td><td>MIPI/LVDS clock Input.</td></tr>
<tr><td>IFSEL[1:0]
(VDDIO)</td><td>Input</td><td>MIPI/LVDS Interface selection..
<table>
<tr><th>IFSEL1</th><th>IFSEL0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>MIPI 3Lane</td></tr>
<tr><td>0</td><td>1</td><td>LVDS</td></tr>
<tr><td>1</td><td>0</td><td>MIPI 4Lane(Default)</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>LNSW[1:0]
(VDDIO)</td><td>Input</td><td>MIPI data lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">MIPI Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>01</td><td>D2</td><td>D1</td><td>CLK</td><td>D0</td><td>D3</td></tr>
<tr><td>10</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>11</td><td>D3</td><td>D0</td><td>CLK</td><td>D1</td><td>D2</td></tr>
</table>
Note: MIPI data lane sequence are used when IFSEL[1:0]=[0:0],[1:0]

LVDS data/clk lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">LVDS Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>01</td><td>D0</td><td>D1</td><td>D2</td><td>CLK</td><td>D3</td></tr>
<tr><td>10</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>11</td><td>D3</td><td>CLK</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>
Note: LVDS data lane sequence are used when IFSEL[1:0]=[0:1]</td></tr>
<tr><td>PNSW
(VDDIO)</td><td>Input</td><td>MIPI/LVDS polarity selection pins. Normally pull low.
<table>
<tr><th rowspan="2">PNSW</th><th colspan="5">Lane Mapping</th></tr>
<tr><th>D0P/N</th><th>D1P/N</th><th>CLKP/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>RES[2:0]
(VDDIO)</td><td>Input</td><td>Panel resolution setting selection: Normally pull high
MIPI or LVDS interface :
<table>
<tr><th>RES[2]</th><th>RES[1]</th><th>RES[0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>800RGBx600</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>960RGBx640</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1024RGBx600</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1280RGBx800</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1366RGBx768</td></tr>
</table>
Note:
MIPI/LVDS mode : RES[2:0] setting only for resolution function,
Zigzag panel structure setting depend on ZIGZAG & ZTYPE pin selection(Select by pin or OTP)
Vertical display line set by internal OTP</td></tr>
<tr><td>DIR
(VDDIO)</td><td>Input</td><td>The shift direction of device internal shift register is controlled by this as shown below : Normally pull high
<table>
<tr><th>DIR</th><th>Function</th></tr>
<tr><td>H</td><td>EIO1→OUT[0,1,2]→・・・→OUT[2049,2050,2051]→EIO2</td></tr>
<tr><td>L</td><td>EIO2→OUT[2049,2050,2051]→・・・→OUT[0,1,2]→EIO1</td></tr>
</table></td></tr>
<tr><td>CS_SD
(VDDIO)</td><td>Input</td><td>Source charge sharing selection : Normally pull low
<table>
<tr><th>CS_SD</th><th>Function</th></tr>
<tr><td>H</td><td>Enable source charge sharing</td></tr>
<tr><td>L</td><td>Disable source charge sharing</td></tr>
</table></td></tr>
<tr><td>CS_GIP
(VDDIO)</td><td>Input</td><td>GIP charge sharing selection: Normally pull low
<table>
<tr><th>CS_GIP</th><th>Function</th></tr>
<tr><td>H</td><td>Enable GIP charge sharing</td></tr>
<tr><td>L</td><td>Disable GIP charge sharing</td></tr>
</table></td></tr>
<tr><td>REV
(VDDIO)</td><td>Input</td><td>Controls whether the data of D0~D2 are inverted or not, Normally pull low. When “REV”=1 these data will be inverted. EX. “00”→“ 3F”, “07”→“ 38”, “15”→“2A”, and so on.</td></tr>
<tr><td>OP_DRV[1:0]
(VDDIO)</td><td>Input</td><td>Source OP driving selection:
<table>
<tr><th>OP_DRV[1]</th><th>OP_DRV[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>75%</td></tr>
<tr><td>0</td><td>1</td><td>100%</td></tr>
<tr><td>1</td><td>0</td><td>125%</td></tr>
<tr><td>1</td><td>1</td><td>133%</td></tr>
</table></td></tr>
<tr><td>DVCOM_WP
(VDDIO)</td><td>Input</td><td>Write protection for internal OTP. Normally High-Z
<table>
<tr><th>DVCOM_WP</th><th>Function</th></tr>
<tr><td>H</td><td>Enable write protect (default)</td></tr>
<tr><td>L</td><td>Disable write protect</td></tr>
</table></td></tr>
<tr><td>DVCOM_EN
(VDDIO)</td><td>Input</td><td>DVCOM selection: Normally pull low
<table>
<tr><th>DVCOM_EN</th><th>Function</th></tr>
<tr><td>H</td><td>Enable DVCOM</td></tr>
<tr><td>L</td><td>Disable DVCOM (VCOM input from external power)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>GIP_LRSEL[1:0]
(VDDIO)</td><td>Input</td><td>GIP Level shift selection : Normally pull high
<table>
<tr><th>GIP_LRSEL[1]</th><th>GIP_LRSEL [0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Disable GIP level shift function</td></tr>
<tr><td>0</td><td>1</td><td>Enable GIP level shift on left side(right off)</td></tr>
<tr><td>1</td><td>0</td><td>Enable GIP level shift on right side(left off)</td></tr>
<tr><td>1</td><td>1</td><td>Enable GIP level shift on left and right side</td></tr>
</table>
Note:
GATE_SW[1:0]=[0:0] disable GIP level shift.(GIP signal pull low)</td></tr>
<tr><td>GATE_SW[1:0]</td><td>Input</td><td>
<table>
<tr><th>GATE_SW [1]</th><th>GATE_SW [0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>External Gate driver</td></tr>
<tr><td>0</td><td>1</td><td>Internal GIP (Default)</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>INV_SEL[1:0]
(VDDIO)</td><td>Input</td><td>Inversion mode selection: Normally pull low.
<table>
<tr><th rowspan="3">INV_SEL
[1:0]</th><th colspan="4">MIPI/LVDS</th></tr>
<tr><th colspan="2">Cascade mode
(CAS=1)</th><th colspan="2">Dual gate
(CAS=0)</th></tr>
<tr><th>Normal type
(ZIGZAG=0)</th><th>Zigzag type
(ZIGZAG=1)</th><th>Normal type
(ZIGZAG=0)</th><th>Zigzag type
(ZIGZAG=1)</th></tr>
<tr><td>00</td><td>1 line</td><td>Column</td><td>1+2dot</td><td>Column</td></tr>
<tr><td>01</td><td>2 line</td><td>Column</td><td>2dot</td><td>Column</td></tr>
<tr><td>10</td><td>1+2line</td><td>Column</td><td>2line2dot</td><td>Column</td></tr>
<tr><td>11</td><td>Column</td><td>Column</td><td>-</td><td>Column</td></tr>
</table>
Note : Four line inversion select by OTP</td></tr>
<tr><td>SCAN_SEL</td><td>Input</td><td>
<table>
<tr><th>SCAN_SEL</th><th>Function</th></tr>
<tr><td>H</td><td>Inverse Z scan : G→R→G→R</td></tr>
<tr><td>L</td><td>Z scan : R→G→R→G(default)</td></tr>
</table>
Note:(Only for Normal dual gate type driving)
Source mapping depend on external gate signal</td></tr>
<tr><td>FRAME</td><td>Input</td><td>Frame inverse or not select. Normally pull low
<table>
<tr><th>FRAME</th><th>Function</th></tr>
<tr><td>H</td><td>Uniform</td></tr>
<tr><td>L</td><td>Frame inverse(default)</td></tr>
</table>
Note: (Only for Normal dual gate type driving)
INV_SEL[1:0]=[1:1] : FRAME pin function is ignored</td></tr>
<tr><td>CAS</td><td>Input</td><td>Cascade mode selection: Normally pull high
<table>
<tr><th>Cascade</th><th>Function</th></tr>
<tr><td>H</td><td>Cascade mode(default)</td></tr>
<tr><td>L</td><td>Dual gate mode</td></tr>
</table>
Refer to application Block diagram</td></tr>
<tr><td>SDLOC</td><td>Input</td><td>Source driver location definition pin. Normally pull high
<table>
<tr><th>SDLOC</th><th>Function</th></tr>
<tr><td>H</td><td>Source driver locate on left side</td></tr>
<tr><td>L</td><td>Source driver locate on right side</td></tr>
</table>
Refer to application Block diagram</td></tr>
<tr><td>ZIGZAG</td><td>Input</td><td>Zigzag driving method setting. Normally pull high
<table>
<tr><th>ZIGZAG</th><th>Function</th></tr>
<tr><td>H</td><td>Zigzag driving method</td></tr>
<tr><td>L</td><td>Normal driving method</td></tr>
</table>
Refer to application Block diagram</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>ZTYPE</td><td>Input</td><td>Zigzag panel layout type selection. Normally pull low
<table><tr><th>ZTYPE</th><th>Function</th></tr><tr><td>H</td><td>Zigzag layout type1</td></tr><tr><td>L</td><td>Zigzag layout type0</td></tr></table>Refer to application Block diagram(only for CAS=H and Zigzag=H)</td></tr>
<tr><td>RESETB
(VDDIO)</td><td>Input</td><td>Global reset pin. Normally pull high.
<table><tr><th>RESETB</th><th>Function</th></tr><tr><td>H</td><td>Normal operation (default)</td></tr><tr><td>L</td><td>The controller is in reset state</td></tr></table>Suggest to connecting with an RC reset circuit for stability.</td></tr>
<tr><td>STBYB
(VDDIO)</td><td>Input</td><td>Standby mode. Normally pull high. STBYB = L, timing controller, source driver will turn off, all output are High-Z.
STBYB = H, normal operation. (Default)</td></tr>
<tr><td>BISTB
(VDDIO)</td><td>Input</td><td>Normal Operation/BIST pattern select. Normally pull high.
<table><tr><th>BISTB</th><th>Function</th></tr><tr><td>H</td><td>Normal operation (default)</td></tr><tr><td>L</td><td>BIST mode</td></tr></table></td></tr>
<tr><td>LVFMT
(VDDIO)</td><td>Input</td><td>8-bit input format select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
<table><tr><th>LVFMT</th><th>Function</th></tr><tr><td>H</td><td>VESA format (default)</td></tr><tr><td>L</td><td>JEIDA format</td></tr></table></td></tr>
<tr><td>LVBIT
(VDDIO)</td><td>Input</td><td>6-bit / 8-bit input select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
<table><tr><th>LVBIT</th><th>Function</th></tr><tr><td>H</td><td>8-bit (default)</td></tr><tr><td>L</td><td>6-bit</td></tr></table></td></tr>
<tr><td>DITHER_EN
(VDDIO)</td><td>Input</td><td>Dithering function enable control. Normally pull low
In LVDS 6-bit mode, IC don’t care DITHER and HFRC setting.
<table><tr><th>DITHER_EN</th><th>Function</th></tr><tr><td>H</td><td>Enable internal dithering function</td></tr><tr><td>L</td><td>Disable internal dithering function</td></tr></table></td></tr>
<tr><td>HFRC_EN
(VDDIO)</td><td>Input</td><td>H-FRC selection. Normally pull low
HFRC = H : H-FRC enable
If “DITHER”=”L”,disable dithering function(HFRC and FRC disable)</td></tr>
<tr><td>CMD_SEL
(VDDIO)</td><td>Input</td><td>Command interface selection. Normally pull high.
<table><tr><th>CMD_SEL</th><th>Function</th></tr><tr><td>H</td><td>I2C (default)</td></tr><tr><td>L</td><td>3-Wire</td></tr></table>MIPI and 3-wire/I2C command can’t receive at the same time.</td></tr>
<tr><td>UPDN
(VDDIO)</td><td>Input</td><td>Gate up or down scan control. Normally pull low.
UPDN = ”L”, STV2 output vertical start pulse and UD pin output logical “L” to Gate driver.
UPDN = ”H”, STV1 output vertical start pulse and UD pin output logical “H” to Gate driver
(only for external gate mode , GIP mode = Dummy)</td></tr>
</table>

Pin Name	Pin Type	Description
A0	Input	Serial interface (I2C) Compatible Device Address Bit 0 input. **Normally pull high.**
LEDON	Output	Back-light enable signal.
LEDPWM	Output	This pin is connected to the external LED driver. PWM type control signal for brightness of the LED backlight. If not used, please float this pin.
CSB (VDDIO)	Input	Serial communication enables. **Normally pull high**
SCL (VDDIO)	Input	Serial communication clock input.
SDA (VDDIO)	I/O	Serial communication data input.
SCL_I2C (VDDIO)	Input	Serial communication clock input.
SDA_I2C (VDDIO)	I/O	Serial communication data input.

Panel driver output

S[2051:0] — Output

Source output mapping with different resolution.
Source output control by RES[2:0] pin define

On Dual gate mode : CAS=0

Resolution	Source channel	Disable channel
1366RGBx768	S[2051:0]	-
1280RGBx800	S[959:0] and S[2051:1092]	S[1091:960]
1024RGBx600	S[767:0] and S[2051:1284]	S[1283:768]
960RGBx640	S[719:0] and S[2051:1332]	S[1331:720]
800RGBx600	S[599:0] and S[2051:1452]	S[1451:600]

On Cascade mode : CAS=1(single gate)

Resolution	Chip on left side		Chip on right side	
	Source channe	Disable channel	Source channel	Disable channel
1366RGBx768	S[2051:0]	-	S[2051:0]	-
1280RGBx800	S[959:0] and S[2051:1092]	S[1091:960]	S[959:0] and S[2051:1092]	S[1091:960]
1024RGBx600	S[767:0] and S[2051:1284]	S[1283:768]	S[767:0] and S[2051:1284]	S[1283:768]
960RGBx640	S[719:0] and S[2051:1332]	S[1331:720]	S[719:0] and S[2051:1332]	S[1331:720]
800RGBx600	S[599:0] and S[2051:1452]	S[1451:600]	S[599:0] and S[2051:1452]	S[1451:600]

Note:
Chip position refer to application Block diagram

GOUTL[1]~ GOUTL[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.
GOUTR[1]~ GOUTR[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.

Power		
VDD	PI	A power supply for analog circuit. VDD=2.3V to 3.6V
VDDIO	PI	A power supply for the I/O circuit. VDDIO=2.3V to 3.6V
VDD_18V	PO	Internal power supply for logic circuits. Connect to a stabilizing capacitor.
VDD_18V_IF	PO	Internal power supply for MIPI circuits. Connect to a stabilizing capacitor.
VDD_IF	PI	Interface and I/O power supply for the MIPI power regulator circuits. VDDIO=2.3V to 3.6V. .
VSS	PI	GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSS_IF	PI	Ground for interface.
VSSA	PI	Analog ground. VSS=0V. When using the COG method, connect to VSS on the FPC to prevent noise.
VSP	PI	Input voltage from the set-up circuit (4.5V to 6.0V).
VSN	PI	Input voltage from the set-up circuit (-4.5V to -6.0V).
VGMP	PO	Positive regulated voltage output (3.728V to 5.76V)
VGMN	PO	Negative regulated voltage output (-3.728V to -5.76V)
VGH	PI	Connect to stabilizing capacitor between VSSA and VGH.
VGL	PI	Connect to stabilizing capacitor between VSSA and VGL.
VGH_REG	PO	Regulator output voltage generated from VGH. Connect to a stabilizing capacitor between VSSA and VGH_REG. If not used, please open.
VGL_REG	PO	Regulator output voltage generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL_REG. If not used, please open.
VCL	PO	Input voltage from the set-up circuit (-3.0V). It is generated from VSN.
VCOM	PO	The power supply of common voltage in DC com driving. The voltage range is set between -0.55V~to -2.46V. It must connected a stabilizing capacitor 2.2u to VSS.

Other pins		
PASS1_R/PASS2_R	-	Pass line
PASS1_L/PASS2_L	-	Pass line
SYNC_L[8:0]	I/O	Sync signal for IC control. (for MIPI/LVDS cascade mode) **Refer to application Block diagram**
SYNC_R[8:0]	I/O	Sync signal for IC control. (for MIPI/LVDS cascade mode) **Refer to application Block diagram**
T_S[114]/T_S[115]	O	Source channel output pin.
T_S[1195]/T_S[1196]	O	Source channel output pin.
DUMMY	T	Test pin. Float these pins for normal operation.
TP[73:0]	T	Test pin. Float these pins for normal operation.
T_VTSEN[2:0]	T	Test pin. Float these pins for normal operation.

Note: P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

6.2 Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Source wiring:

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VDD	< 5	T_VTSEN[2]	< 100
VDD_IF	< 5	T_VTSEN[1]	< 100
VDDIO	< 5	T_VTSEN[0]	< 100
VDD_18V	< 5	DUMMY	< 100
VDD_18V_IF	< 5	SHIELDING	< 100
VSP	< 5	DP[0]/DN[0]	< 5
VSN	< 5	DP[1]/DN[1]	< 5
VGH	< 5	DP[2]/DN[2]	< 5
VGL	< 5	DP[3]/DN[3]	< 5
VGMP	< 5	CKP/CKN	< 5
VGMN	< 5	DIR	<100
VGH_REG	< 5	GOUTR[1]~GOUTR[22]	< 50
VGL_REG	< 5	GOUTL[1]~GOUTL[22]	< 50
VCOM	< 5	SCL	< 50
VSSA	< 5	SDA	< 50
VSS_IF	< 5	SCL_I2C	< 50
VSS	< 5	SDA_I2C	< 50
RES[2:0]	< 100	VCL	< 5
STBYB	< 100	CMD_SEL	< 100
RESETB	< 100	LNSW[1:0]	< 100
PNSW	< 100	GATE_SW[1:0]	< 100
REV	< 100	SYNC_R[1]~SYNC_R[7]	< 100
LVFMT	< 100	SYNC_L[1]~SYNC_L[7]	< 100
LVBIT	< 100	UPDN	< 100
IFSEL[1:0]	< 100	CSB	< 50
DVCOM_WP	< 100	TP	<100
CS_SD	< 100		
CS_GIP	< 100		
BISTB	< 100		
LEDPWM	< 50		
LEDON	< 50		

7. Register Command Format

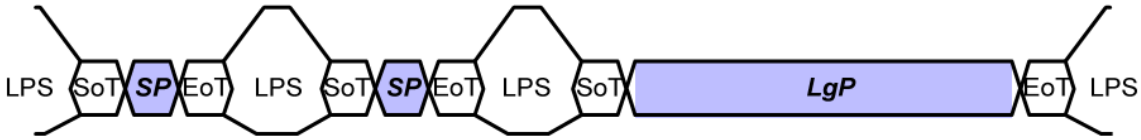
The EK79202 supports set internal register by MIPI interface and I2C interface. MIPI and I2C interface use different register address. The MSB bit [7] of address is only for MIPI interface. The SPI and I2C must be ignored its. “MIPI address” and “SPI/I2C address” showed in register table.

7.1 MIPI command mode control register

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. The diagram illustrates as multiple packets being sent separately, and as concatenated packets in a single HS transmission.

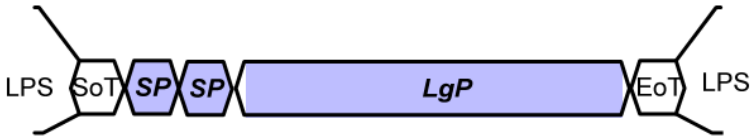
In HS Mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT between packets. This constraint does not apply to LP transmissions



Separate Transmissions

KEY:

LPS	– Low Power State	SP	– Short Packet
SoT	– Start of Transmission	LgP	– Long Packet
EoT	– End of Transmission		



Single Transmission

7.2 I2C format

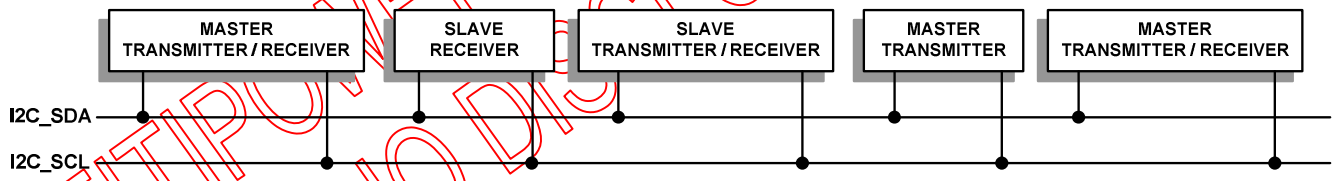
The I^{2}C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I^{2}C_SDA) and the Serial Clock Line (I^{2}C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I^{2}C-Bus Protocol:

Before any data is transmitted on the I^{2}C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

(b) Definitions:

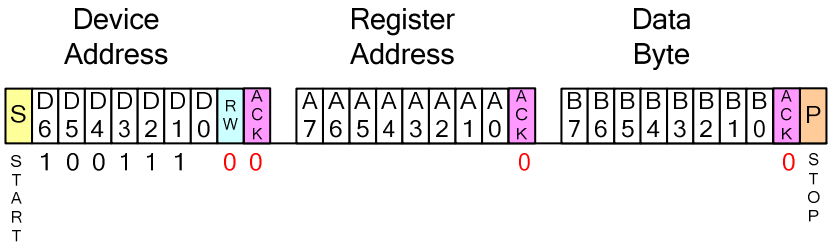
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



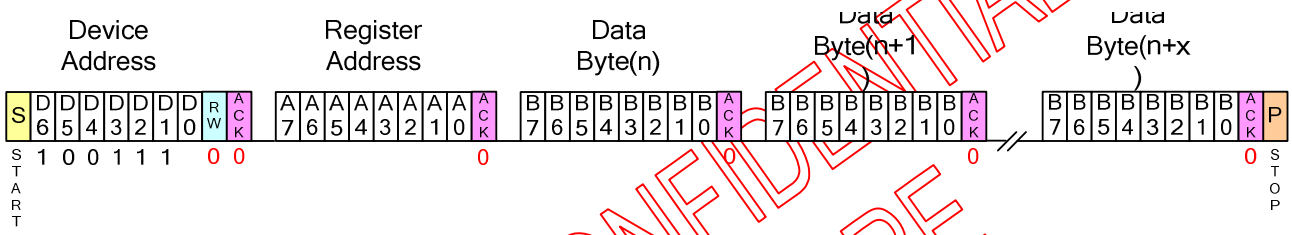
7.3.1 Register Write Sequence of I^{2}C Interface

EK79202 supports register write sequence via I^{2}C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) EK79202 DA[6:0]=100_1111 or DA[6:0]=100_1110



Single Register Writing Timing

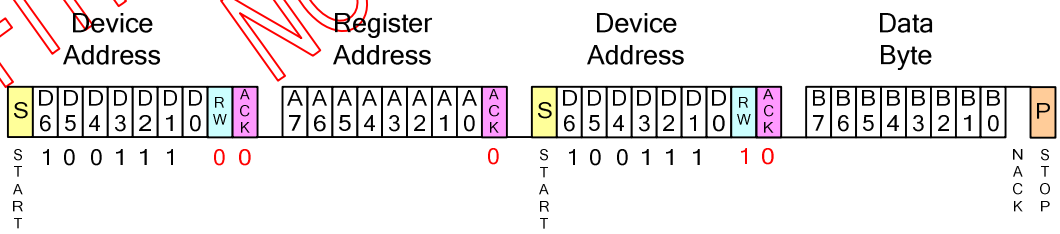


Multi Register Writing Timing

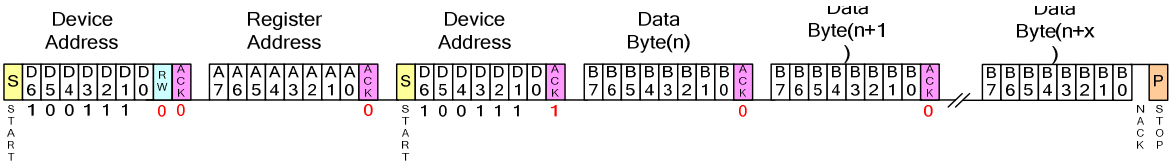
7.3.2 Register Read Sequence of I2C Interface

EK79202 supports register read sequence via I²C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.



Single Register Reading Timing



Multi Register Reading Timing

7.4 SPI format

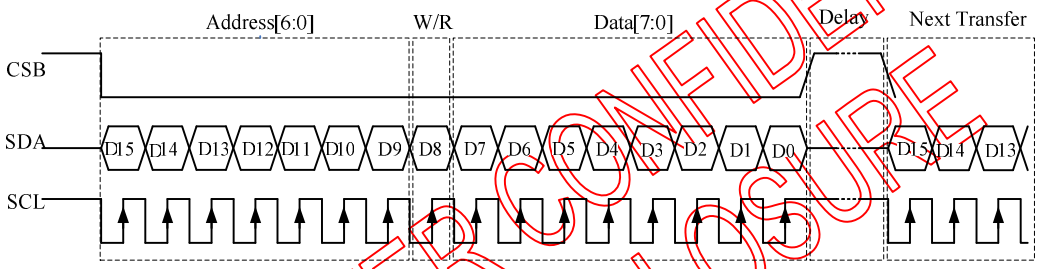
EK79202 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79202 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing. Because the 3-wire only can read/write one address. So we put the “parameter index” at the address 0x2F. When 3-wire command sends, it will refer to the address 0x2F[4:0] as the parameter index value.



3-Wire Command Format:

Bit	Description
D15-D9	Register Address [6:0].
D8	W/R control bit. “0” for Write; “1” for Read
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							0	Data (Issue by external controller)							

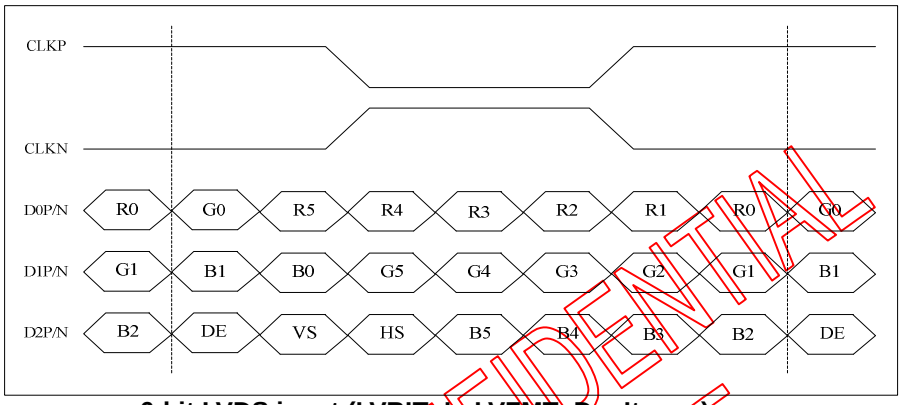
3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							1	Data (Issue by 3-Wire engine)							

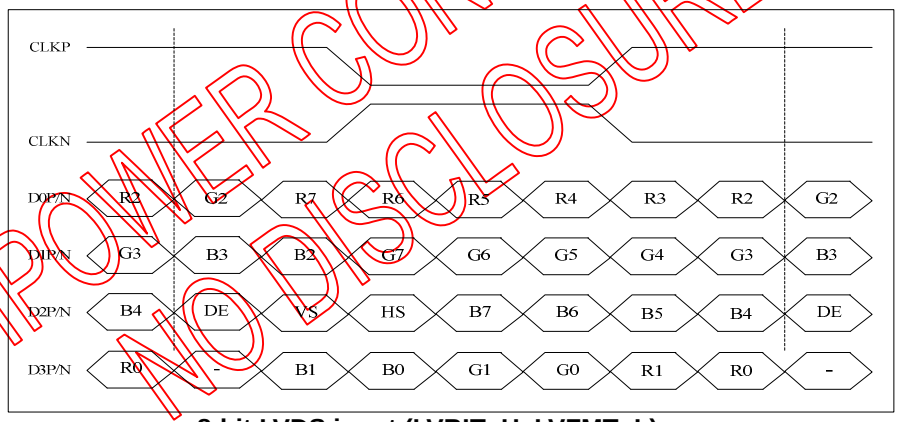
8. Video Interface and Timing Table

8.1 LVDS interface

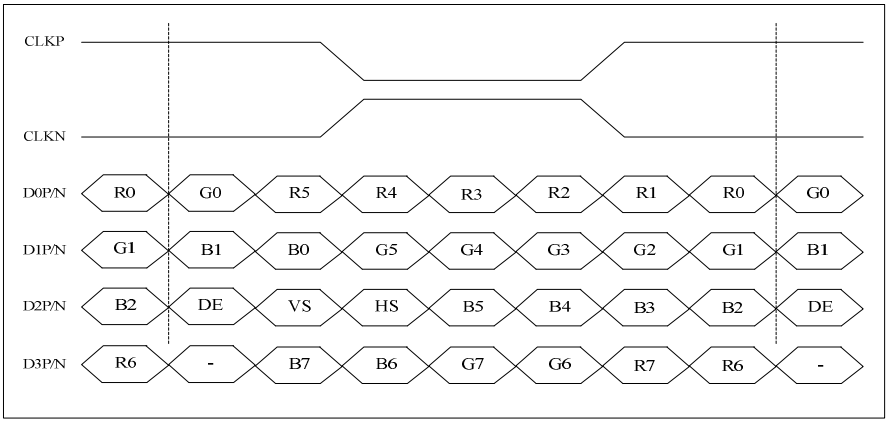
8.1.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

8.1.2 LVDS/MIPI Input Timing Table

For 1366RGBx768

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	69.6	75	80.9	MHz
HSYNC period time		T_H	1466	1550	1596	DCLK
Horizontal display area		T_{HD}		1366		DCLK
HSYNC pulse width	Min.	T_{HPW}		1		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	96	142	DCLK
VSYNC period time		T_V	792	806	840	H
Vertical display area		T_{VD}		768		H
VSYNC pulse width	Min.	T_{VPW}		1		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

For 1280RGBx800

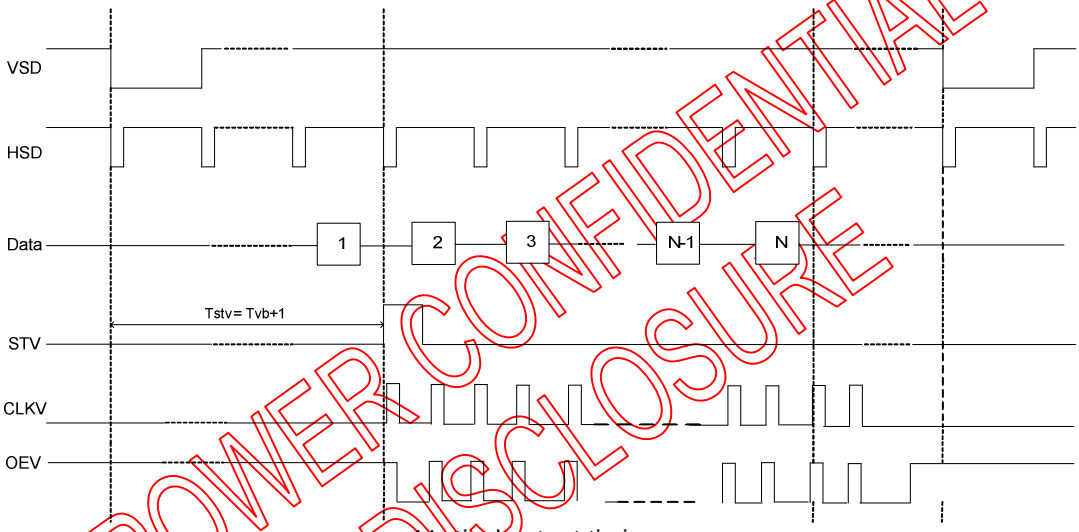
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	66.3	72.4	78.9	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}		1280		DCLK
HSYNC pulse width	Min.	T_{HPW}		1		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
VSYNC period time		T_V	824	838	872	H
Vertical display area		T_{VD}		800		H
VSYNC pulse width	Min.	T_{VPW}		1		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

MIPI Frequency = (Frame rate) x TH x TV x 24bits.
Mini-LVDS (3-pair) = DCLK rate x 3.

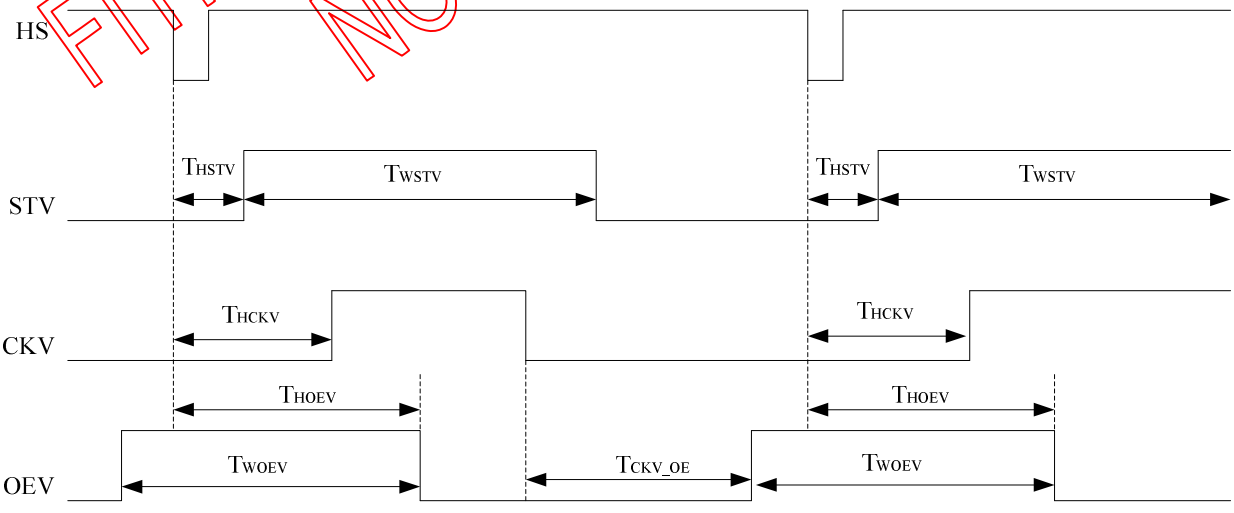
8.1.3 Gate Output Timing Table

(VDD=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STV Pulse Width	T_{WSTV}	-	1	-	H
Time from HSD to STV	T_{HSTV}	-	2	-	DCLK
Time from HSD to CKV	T_{HCKV}	-	25	-	DCLK
Time from HSD to OEV	T_{HOEV}	-	35	-	DCLK
Time from CKV to OEV	T_{CKV_OE}	-	168	-	DCLK
OEV Pulse Width	T_{WOEV}	-	188	-	DCLK



Vertical output timing



Gate output timing

9. Power Sequence and External Power Circuit

9.1 Power Generation

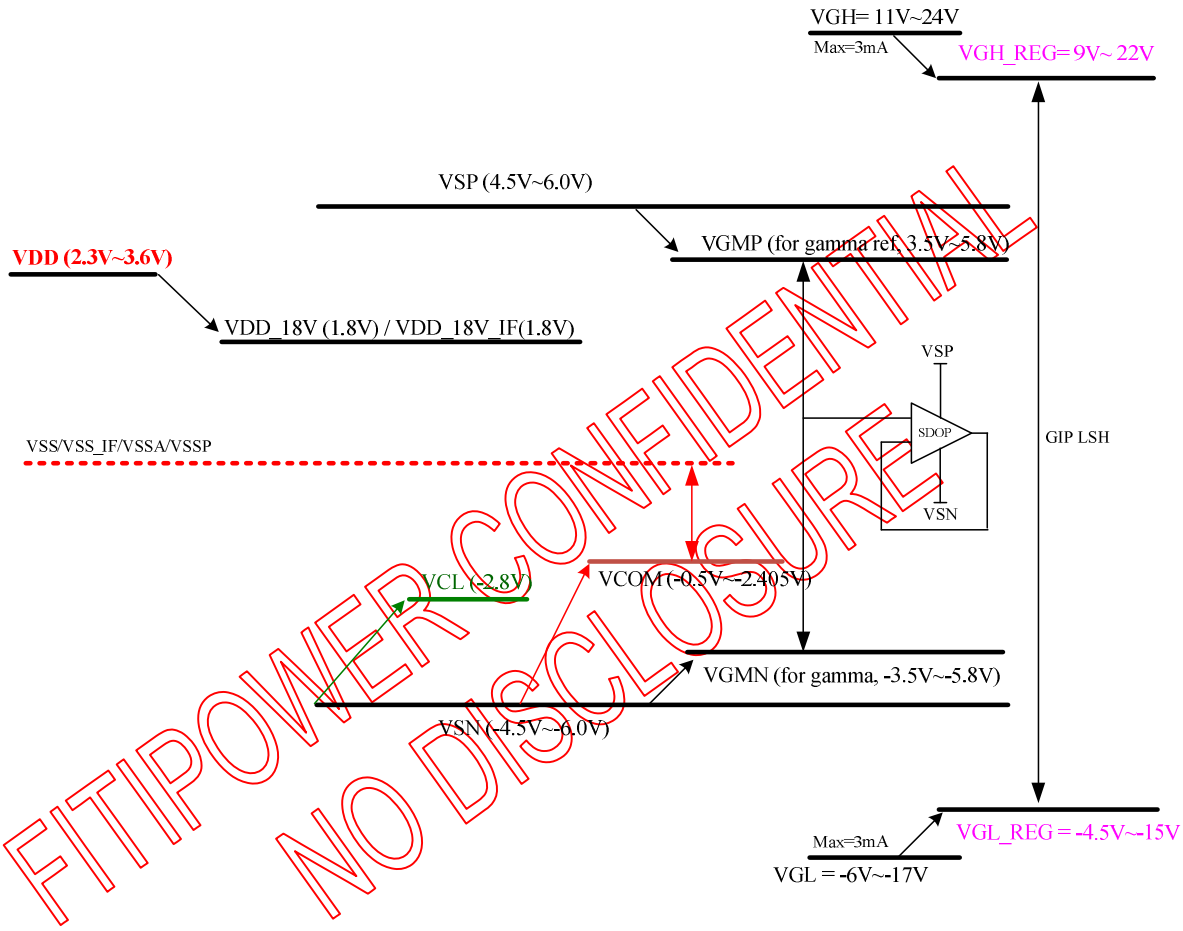
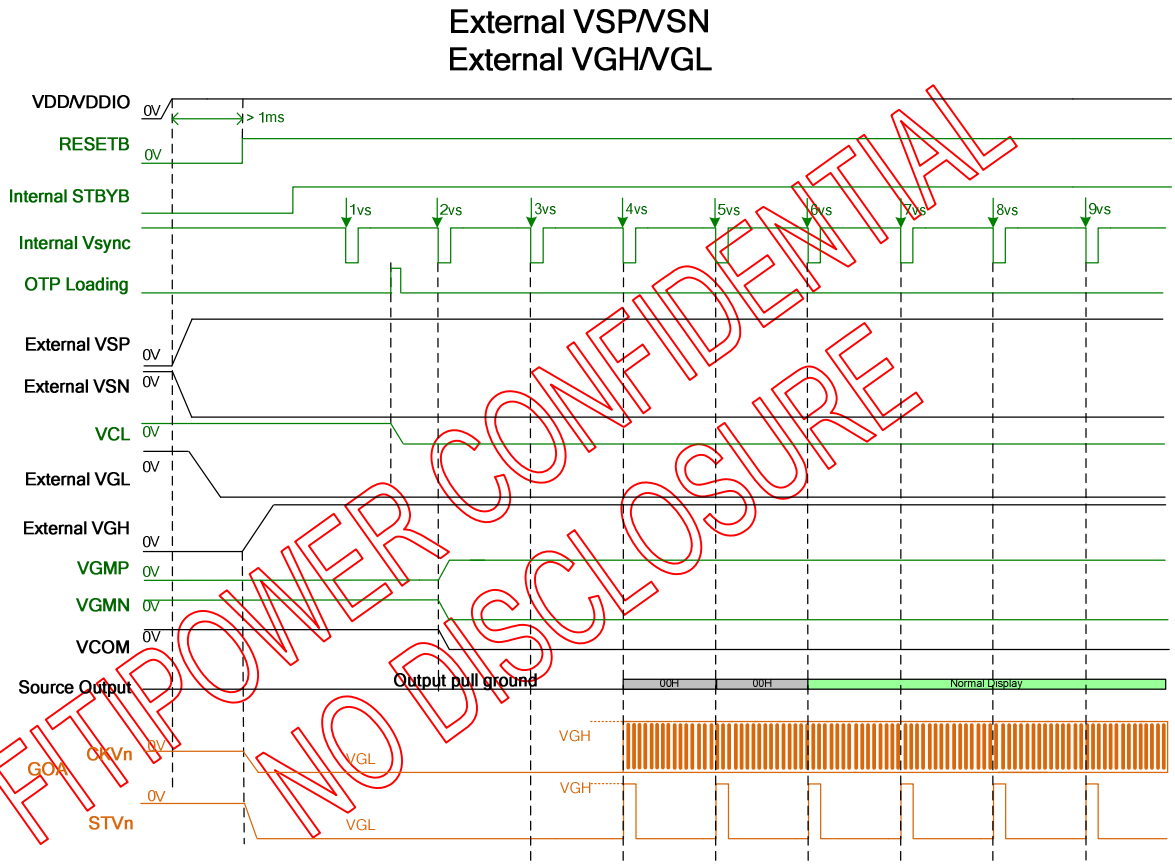


Figure 7.1 power generation

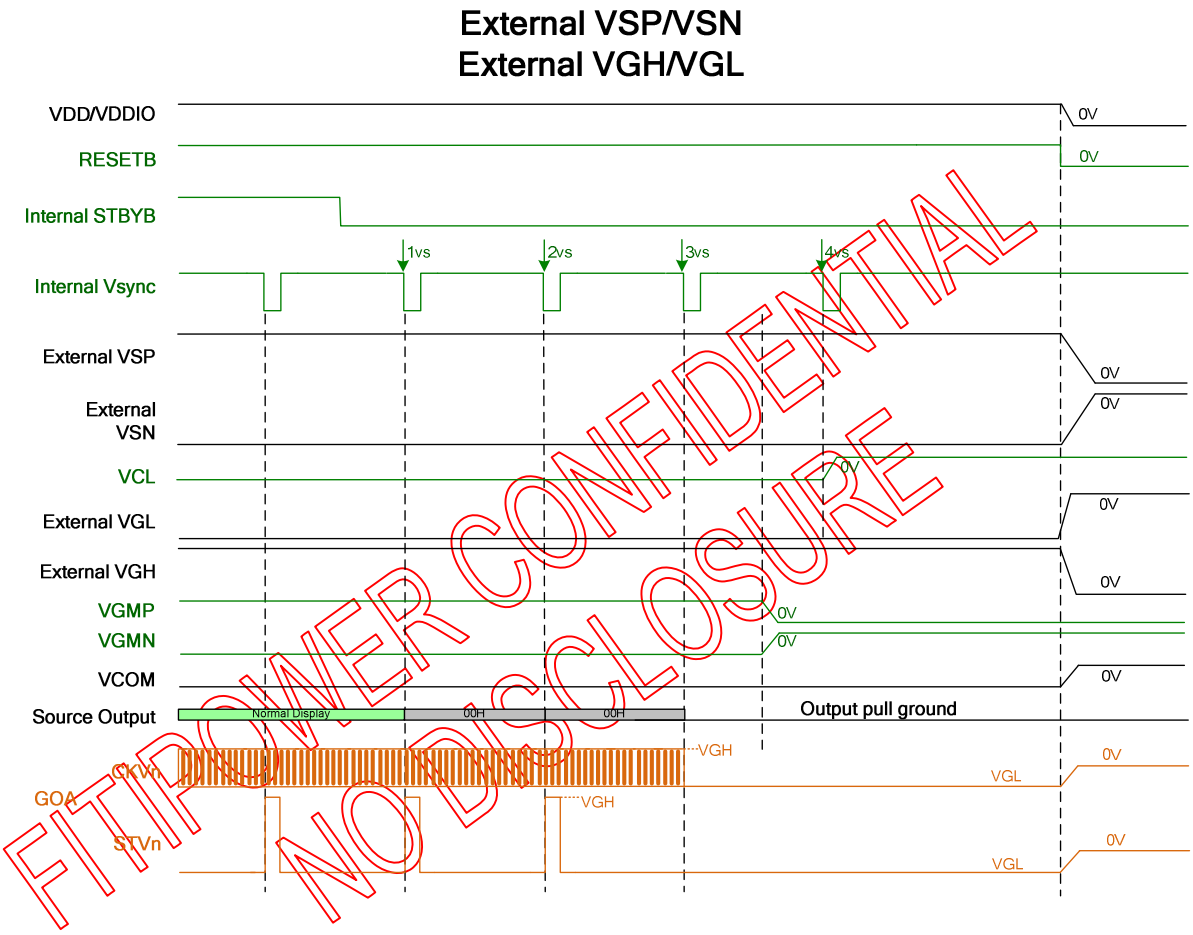
9.2 Power on sequence

9.2.1 Power on sequence



Power on sequence with PMODE=H

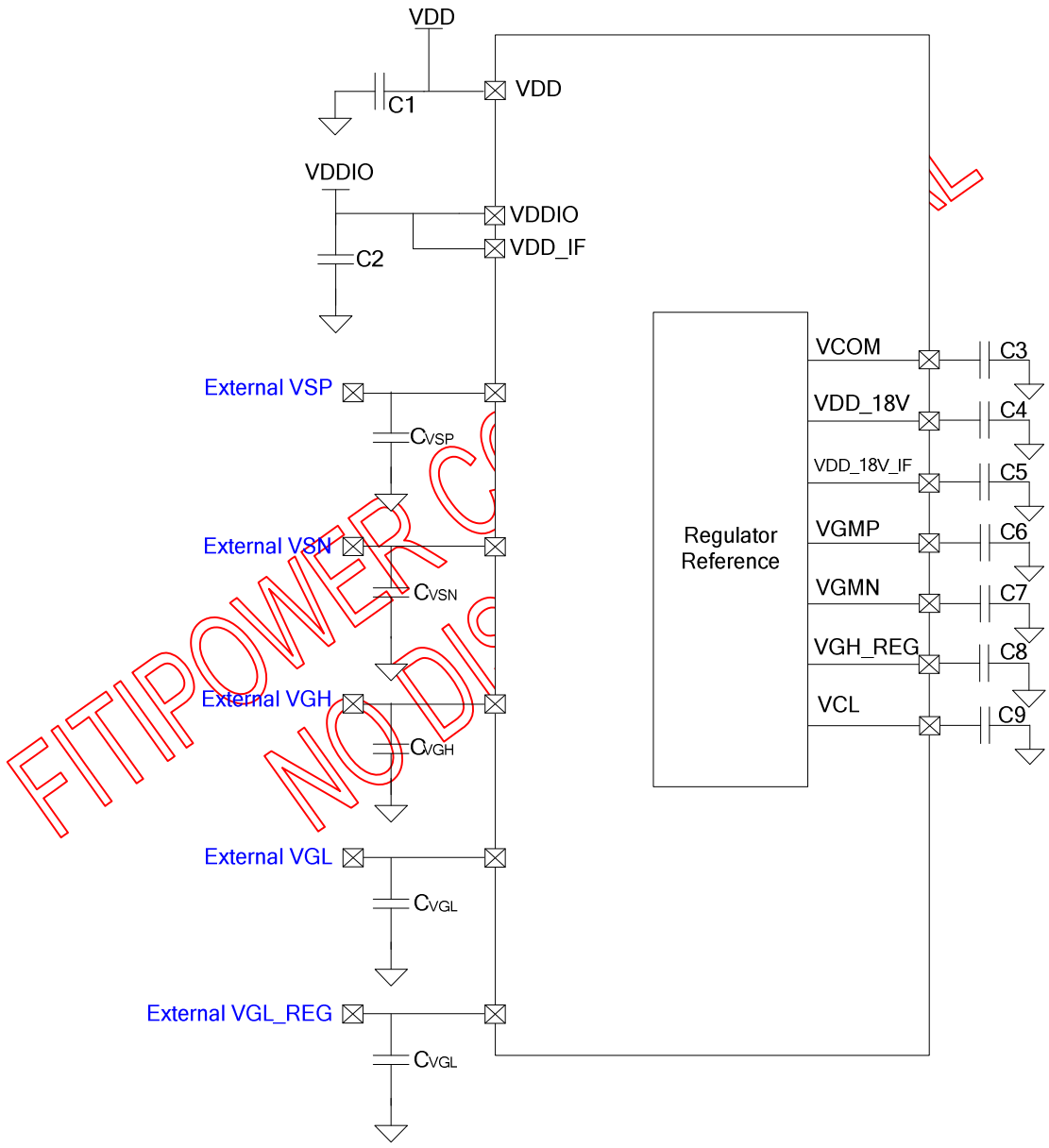
9.2.2 Power off sequence



Power off sequence with PMODE=H

9.3 Application power circuit

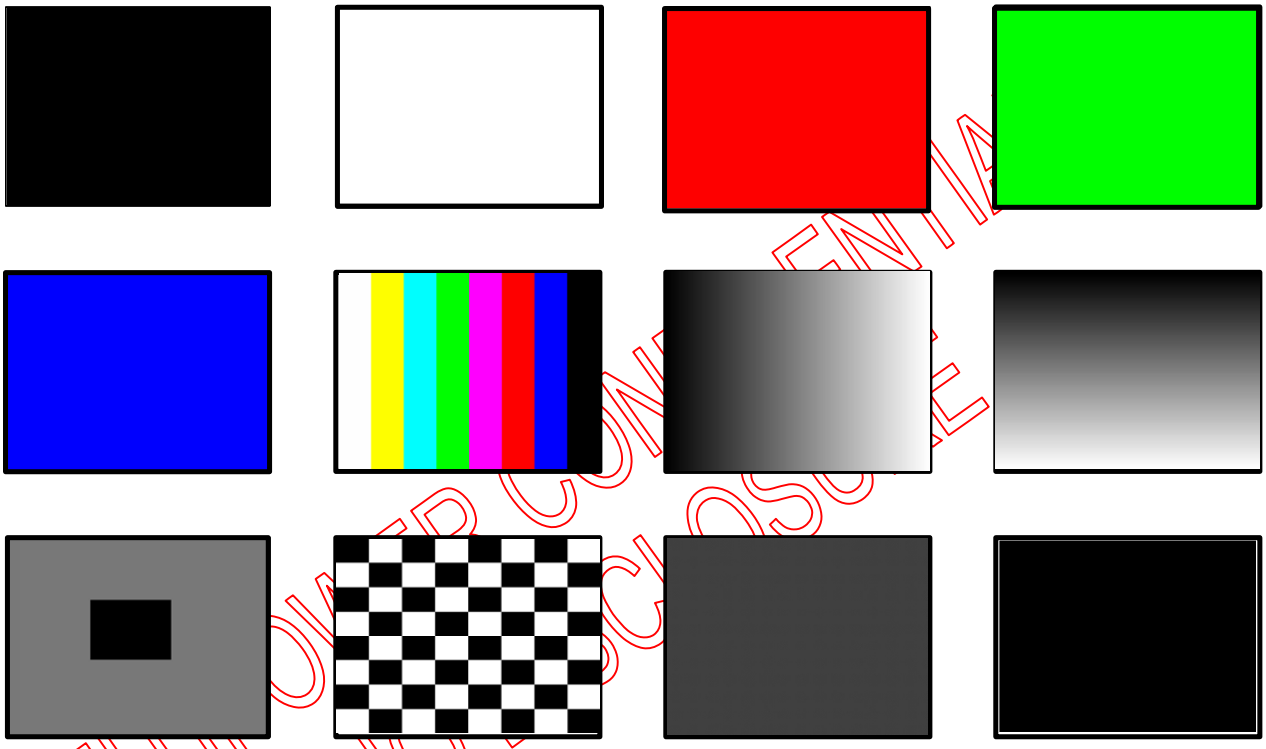
VDD=VDDIO=VDD_IF=2.3~3.6V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



10. Function Description

10.1 BIST pattern

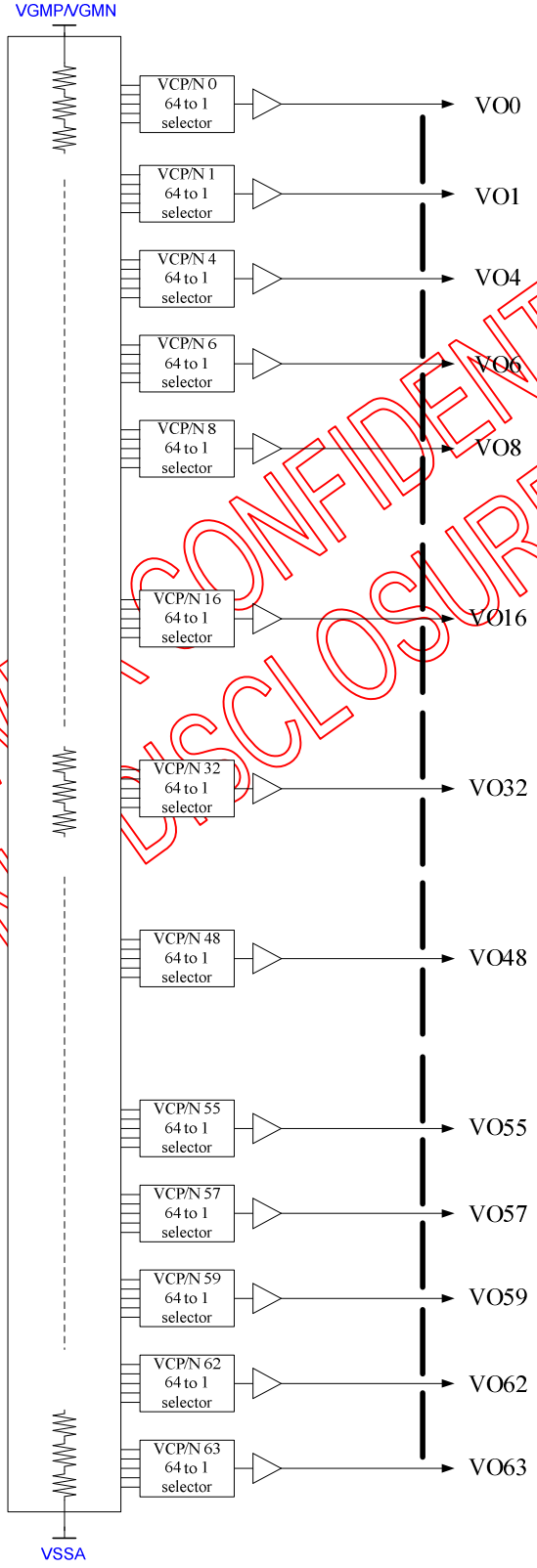
We support the BIST mode to test panel and debug. It can stop pattern at any time while BISTB set to low. The pattern sequence is listed below.



Black→White→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame

11. Gamma Correction Resistances

We use the gamma resistor stream and 64-to-1 selector to adjust voltage

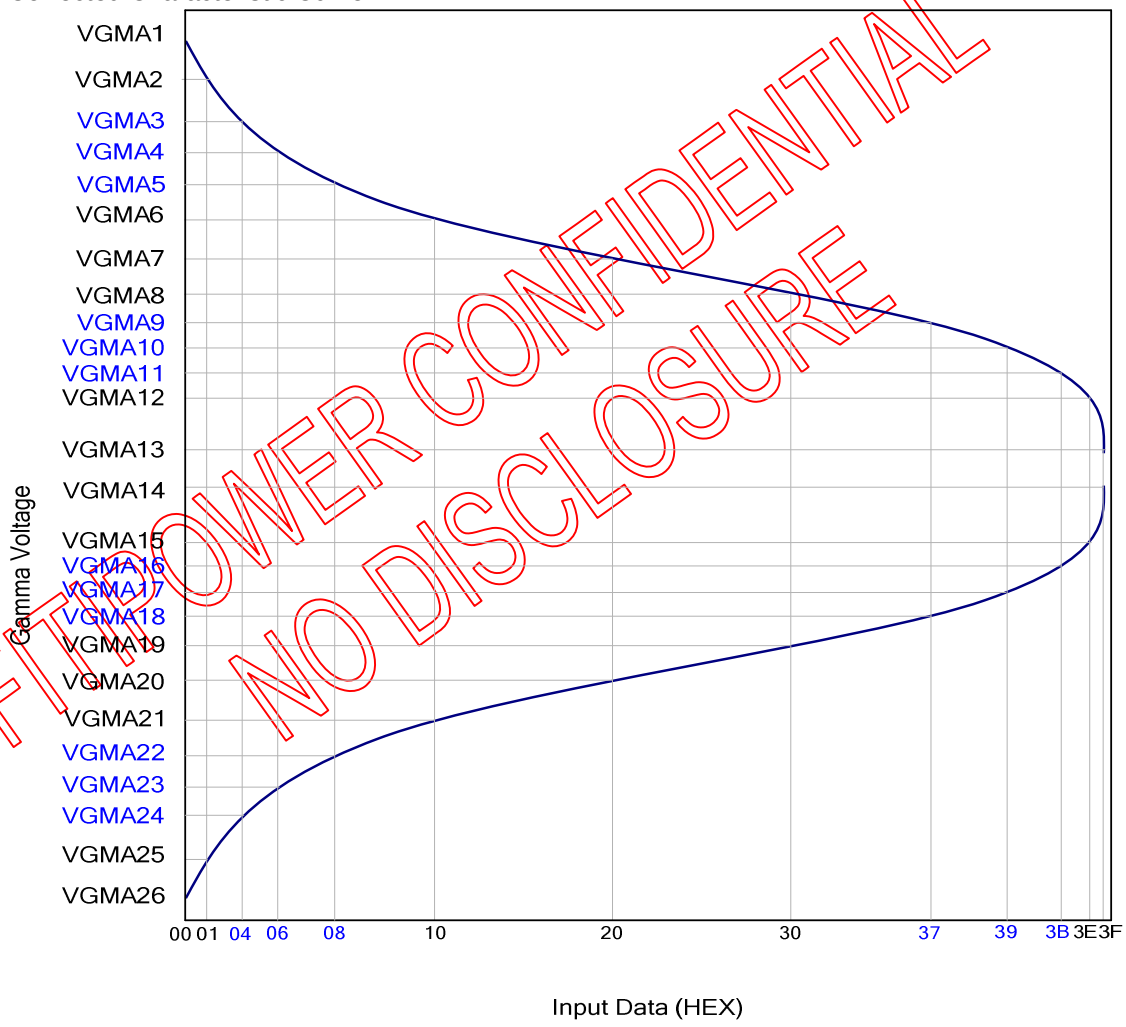


11.1 Relationship between input data and output voltage

The output voltage is determined by the 6-bit digital input data, POL and the 26 gamma corrected reference voltages. Among these gamma corrected reference voltages,VGMA1 ~VGMA13 and VGMA14 ~VGMA26 are for positive polarity voltage output and negative polarity voltage output respectively.

POL	OUT_{2n-1}	OUT_{2n}
H	VGMA14~VGMA26	VGMA1~VGMA13
L	VGMA1~VGMA13	VGMA14~VGMA26

GAMMA Corrected Characteristic Curve



Note:
VSP ≧ VGMP+0.2
VSN ≦ VGMN-0.2
VGMA13-0.2V ≧ GND ≧ VGMA14+0.2V

12. DC Characteristics

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
I/O voltage	VDDIO	2.3	-	3.6	V	
Power input	VDD	2.3	-	3.6	V	
VSP voltage	VSP	4.5	-	6	V	
VSN voltage	VSN	-6	-	-4.5	V	
Operating Temperature		-20	-	85	℃	(1)

Note :(1) Do not let condensation for low temperature

Table 10.1: Absolute maximum rating

12.2 Typical operating condition

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD voltage	VDD	-	3.3	-	V	Analog supply voltage
VDDIO voltage	VDDIO	-	3.3	-	V	I/O Power supply voltage
VSP voltage	VSP	4.5	5.0	6	V	VSP voltage
VSN voltage	VSN	-6	-5.0	-4.5	V	VSN voltage
VGH voltage	VGH	11	18	24	V	VGH voltage
VGL voltage	VGL	-17	-12	-6	V	VGL_ voltage
VGL_REG voltage	VGL_REG	-15	-10	-4.5	V	VGL_REG voltage

Table 10.2: Typical operating conditions

12.3 DC electrical characteristics

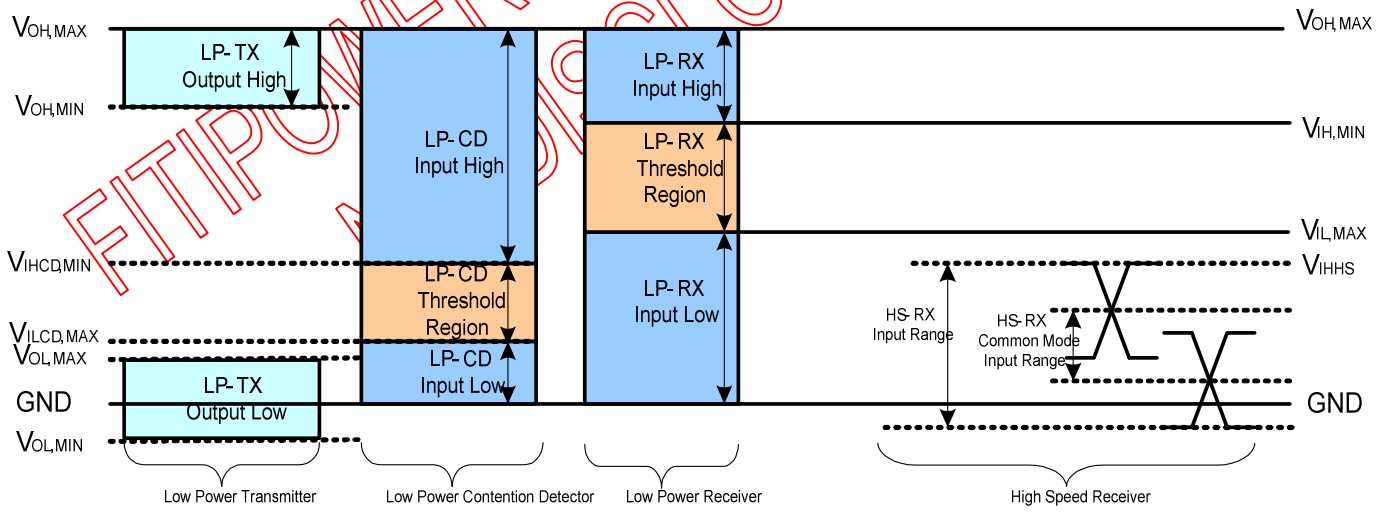
(Test condition: VDD=VDDIO=VDDIF=2.3~3.6V, TA=-20℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
VDDIO Input high level voltage		VIH	0.8 x VDDIO		VDDIO	V	
VDDIO input low level voltage		VIL	VSS		0.2 x VDDIO	V	
Input Leakage Current		Ileak	(-1)		(+1)	μA	
VGH_REG output voltage		VGH_REG	9	16	22	V	
VGL_REG output voltage		VGL_REG	-15	-10	-4.5		
VGMP output voltage		VGMP	3.5	4.24	5.8	V	
VGMN output voltage		VGMN	-5.8	-4.64	-3.5	V	
VGL output voltage		VGL	-17	-12	-6	V	
VGH output voltage		VGH_O	11	18	24	V	
VCL output voltage		VCL	-3	-2.8	-2.1	V	
VCOM output voltage		VCOM	-2.405	-1.5	-0.5	V	
Input terminal resistance		ZID		100		ohm	
Source output level deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255			TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240			TBD		mV	
	Graycode = 32 ~ 207			TBD		mV	
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-		TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-		TBD		mV	
	Graycode = 32 ~ 207	-		TBD		mV	
Current consumption	Analog Operating	IAOP		TBD		mA	
	Analog Stand-by	IAST		TBD		mA	
Rush current		Ivddpeak		TBD		mA	

12.4 MIPI DC electrical characteristics

(VDD=VDDIO=VDD_IF=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-20 to +85℃)

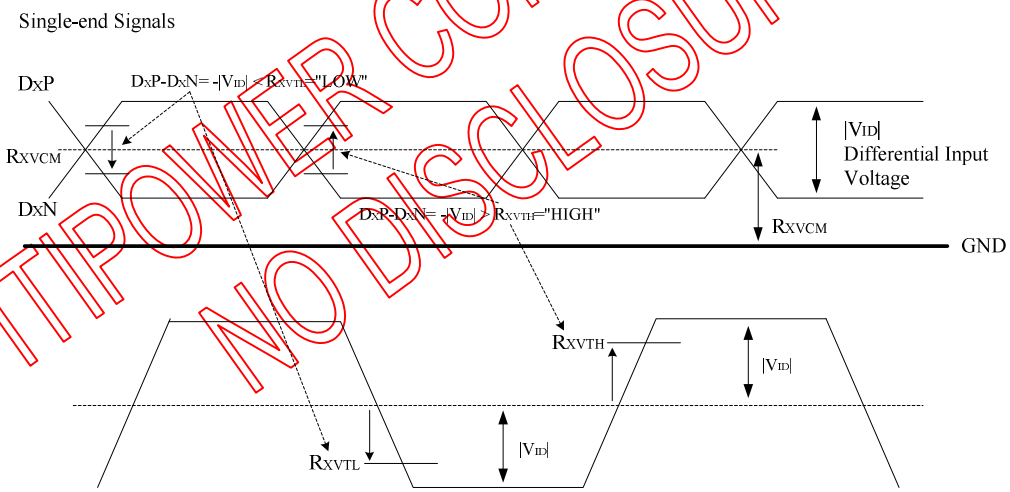
Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
HS transmit differential voltage($V_{OD}=V_{DP}-V_{DN}$)	$\|V_{OD}\|$	100	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	1000	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
MIPI Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA
MIPI Digital Stand-by Current	I_{STMIPI}	-	-	250	uA



12.5 LVDS DC electrical characteristics

(VDD=VDDIO=VDDIF=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{XVTH}	+0.1	0.2	0.3	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-0.3	-0.2	-0.1	V	
Input voltage range (singled-end)	R_{XVIN}	0.7	-	1.7	V	
Differential input common mode voltage	R_{XVCM}	1	1.2	1.4	V	$\|V_{ID}\|$=0.2
Differential input impedance	Z_{ID}	80	100	125	ohm	
Differential input voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Differential input leakage current	I_{LCLVDS}	-10	-	+10	uA	
LVDS Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA	F_{DCLK}=80MHz,VDD=3.3V, Input pattern: 55h->AAh->55h->AAh
LVDS Digital Stand-by Current	I_{STMIPI}	-	-	250	uA	Clock & all Functions are stopped



13. AC Characteristics

13.1 MIPI AC characteristics

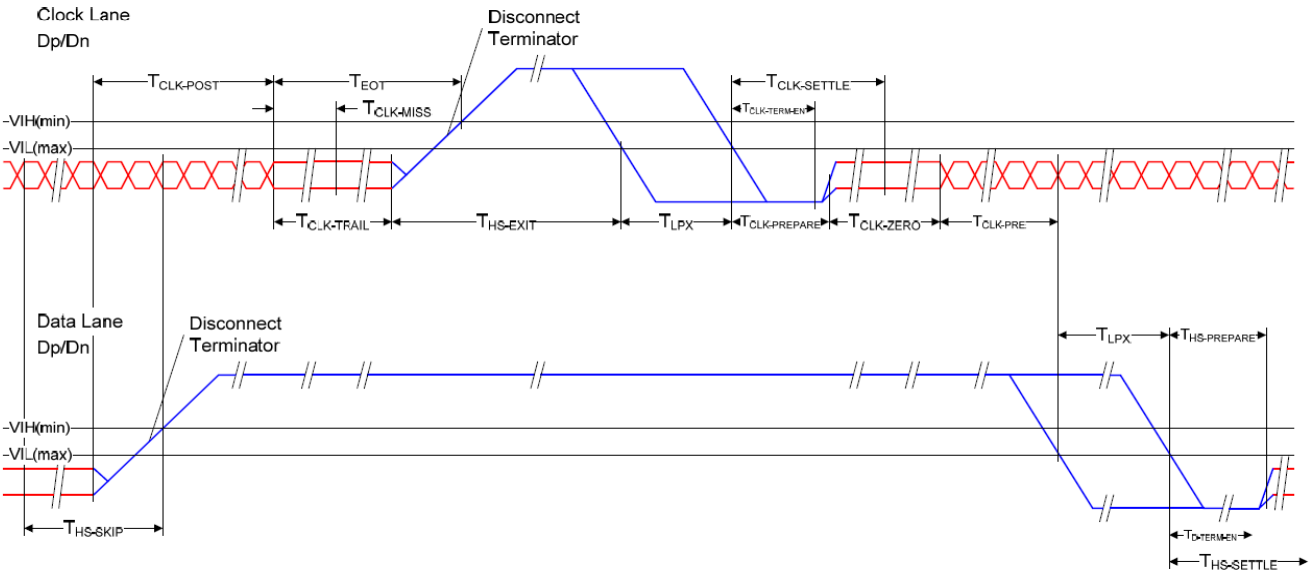


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

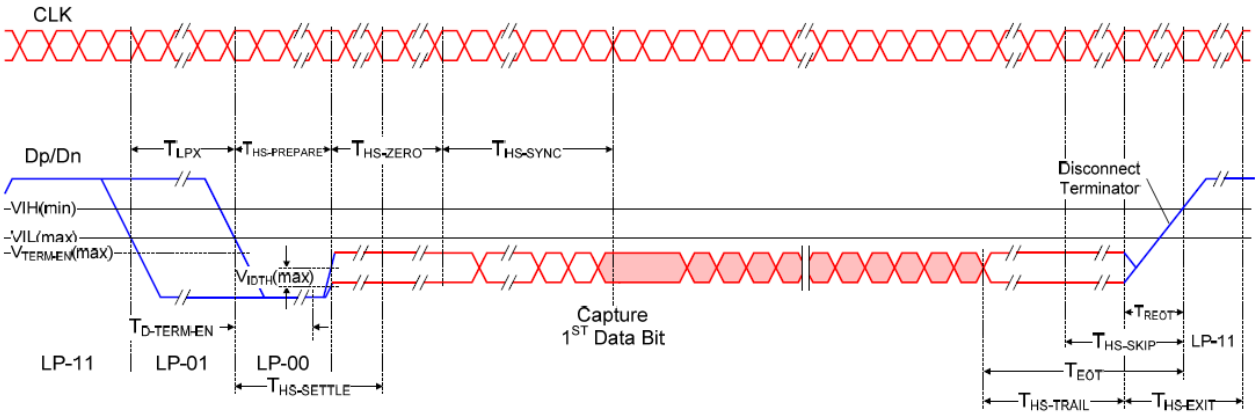


Figure 13.2: Timing of high-speed data transmission in bursts

13.2 MIPI data-clock timing specification

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

13.3 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics

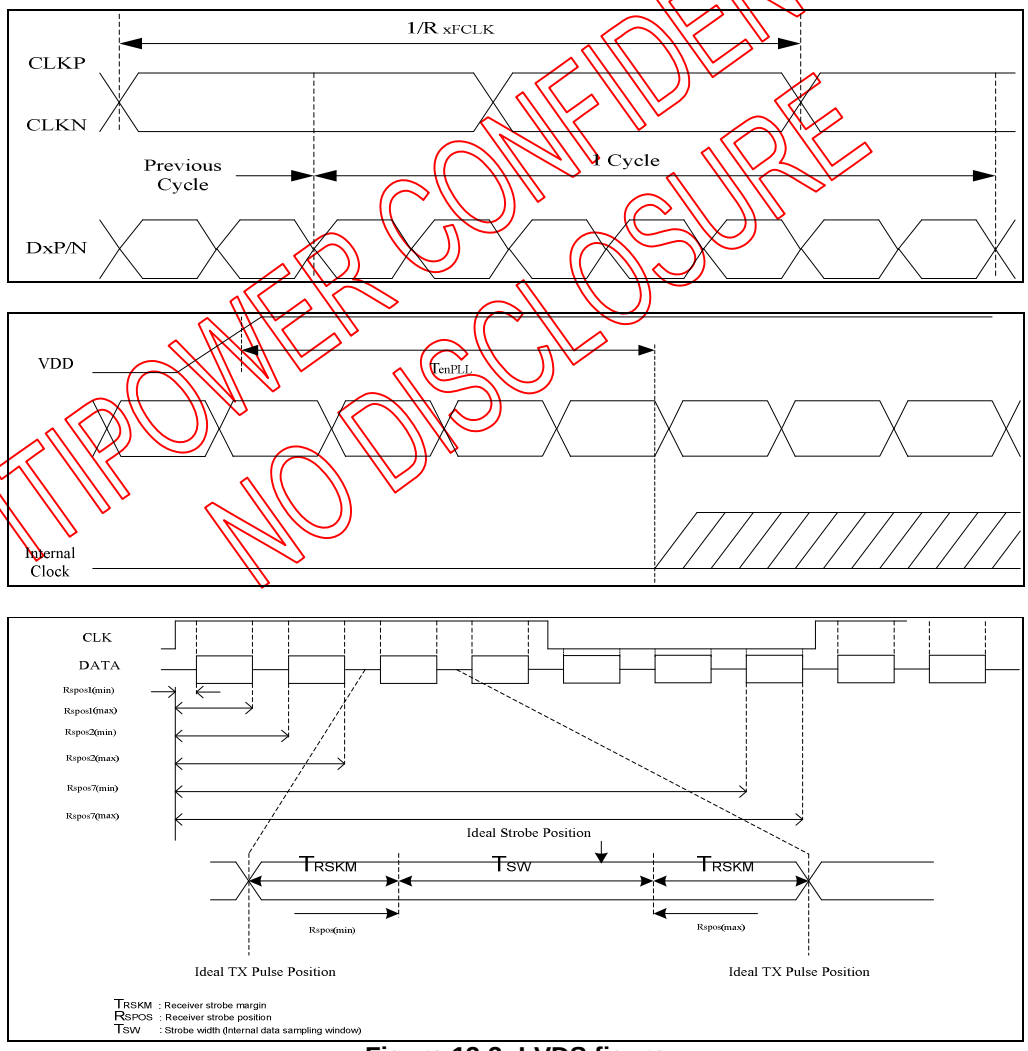
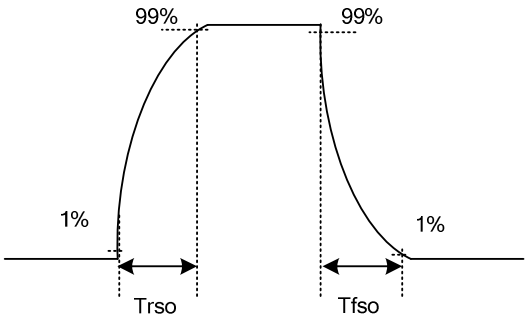
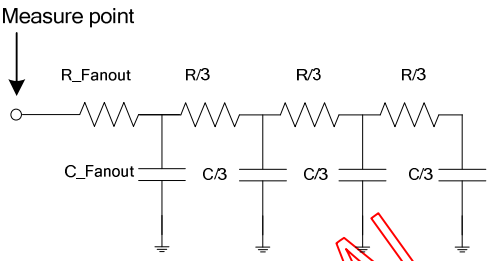


Figure 13.3: LVDS figure

13.4 Source output timing (SOUT0 ~ SOUT2051)



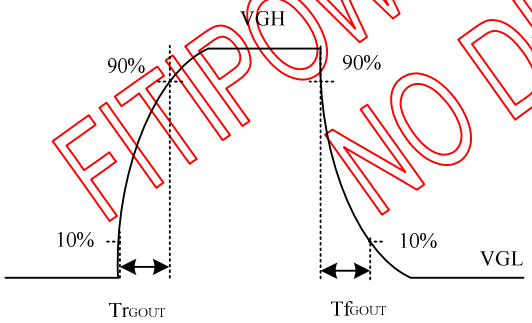


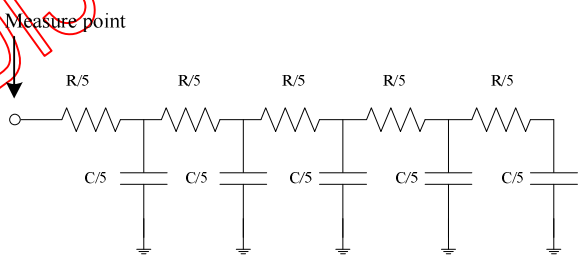
Rdata_total = 25.072k(ohm)
Cdata_total = 83 pF

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Source driver rising time	Trso			3.52		µs
Source driver falling time	Tfso			2.8		µs

Table 13.2: Source output timing

Panel control signal output (GOUTL[1]~GOUTL[22] , GOUTR[1]~GOUTR[22])





Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Panel control signal rising time	T_{rGOUT}	TBD	-	-	TBD	µs
Panel control signal falling time	T_{fGOUT}	TBD	-	-	TBD	µs

Table 13.3: GOA output timing

13.5 Serial interface characteristics

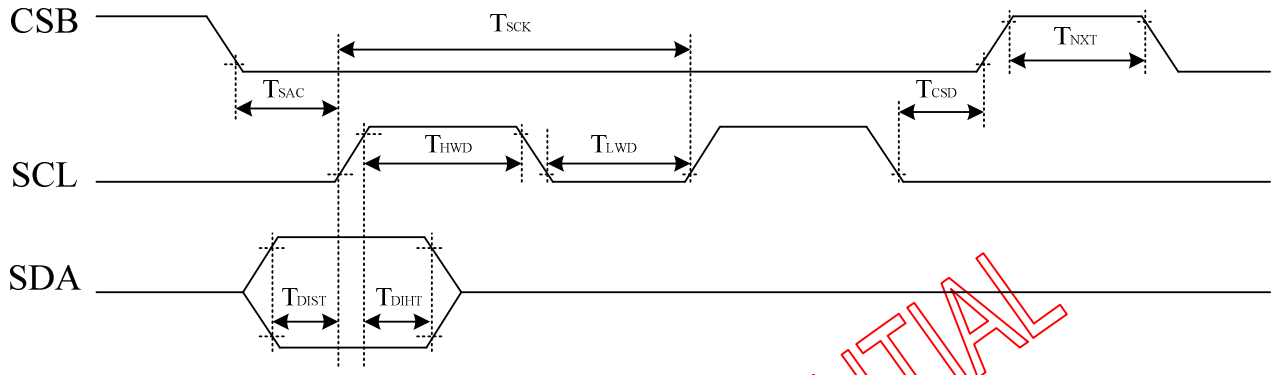


Figure 13.4: Serial interface characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB de-assertion from last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_E		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns

14.6 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=2.3V~3.6V, VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	µs

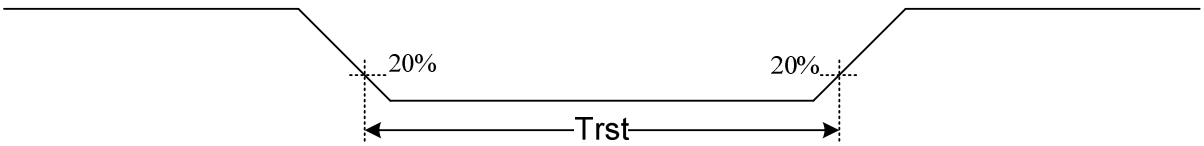
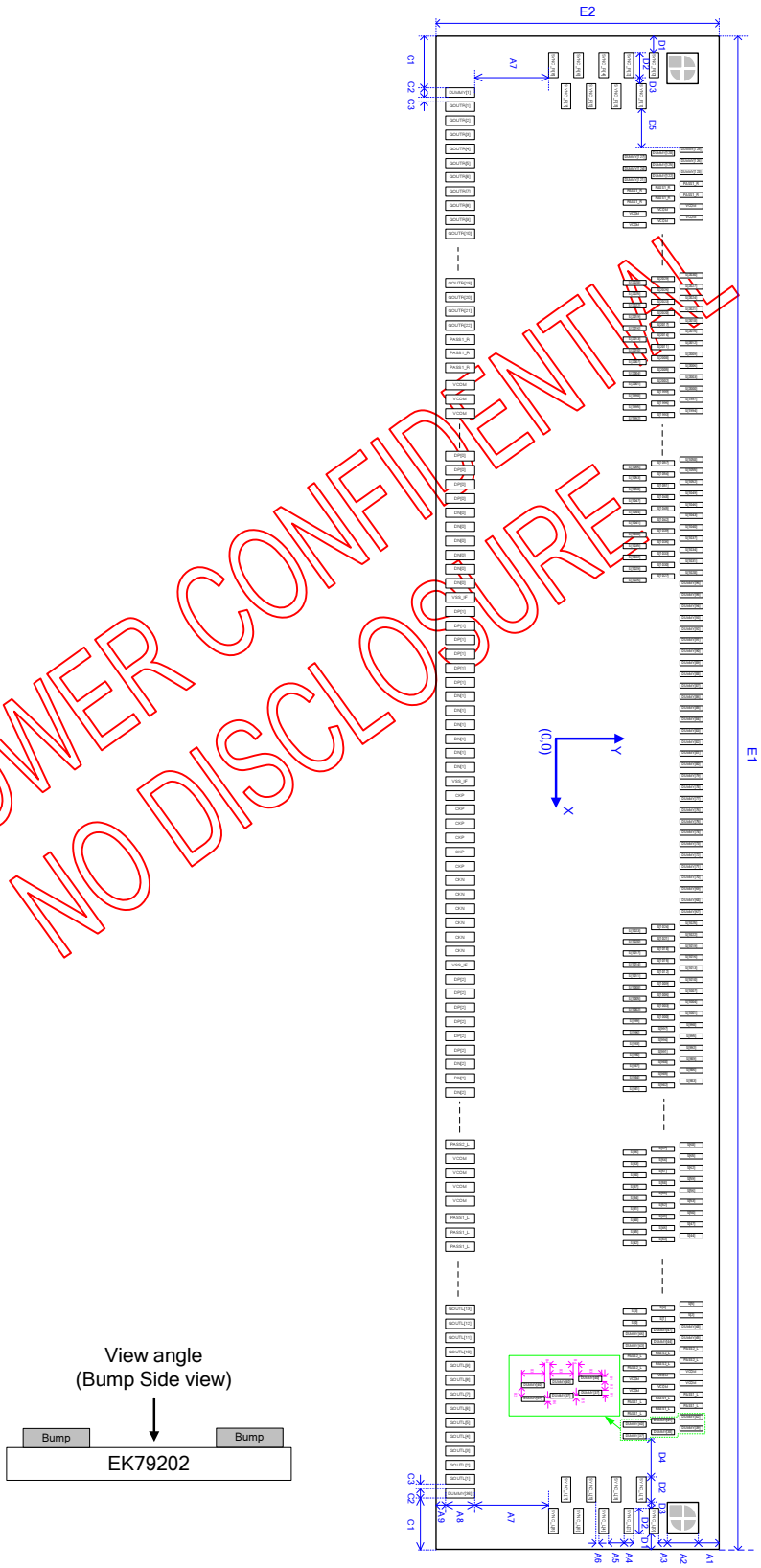


Figure 13.5: Reset timing

14.Chip Outline Dimension



Symbol	Dimension
A1	50
A2	100
A3	31
A4	30
A5	50
A6	10
A7	395
A8	93
A9	41
-	

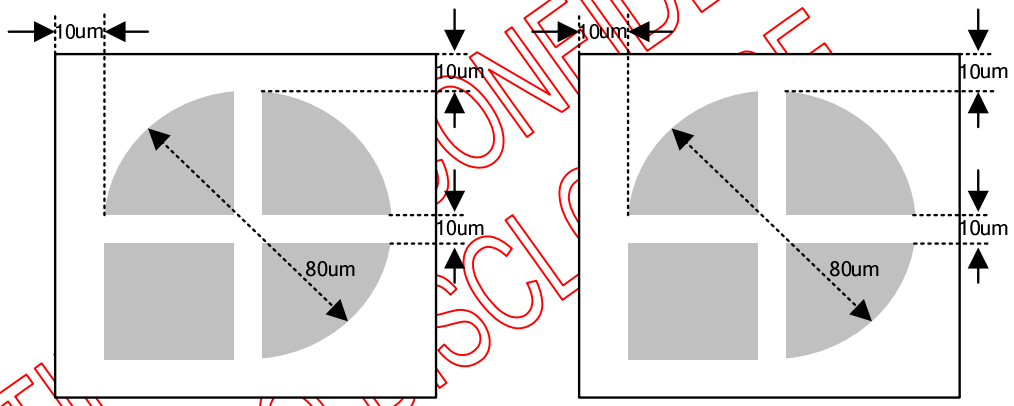
Symbol	Dimension
B1	16
B2	20
B3	73
B4	17
B5	12
B6	12
-	
-	-
-	-
-	-

Symbol	Dimension
C1	163
C2	30
C3	15
-	-
-	-
-	-
-	-
-	-

Symbol	Dimension
D1	50
D2	80
D3	20
D4	122
D5	122
E1	27600
E2	900
-	-
-	-
-	-

Unit : um

14.1 Alignment mark



Alignment mark_R Alignment mark_L

ALM	X - axis	Y - axis
A_MARK_R	-13700	350
A_MARK_L	13700	350

14.2 Pad Corrdinate

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1	SYNC_R[0]	-13706.00	254	58	VGH	-11449.16	-362.5	115	TP[11]	-8884.91	-362.5
2	SYNC_R[1]	-13606.03	214	59	VGH	-11404.17	-362.5	116	TP[12]	-8839.92	-362.5
3	SYNC_R[2]	-13706.00	174	60	VGH	-11359.18	-362.5	117	TP[13]	-8794.93	-362.5
4	SYNC_R[3]	-13606.03	134	61	VGH	-11314.20	-362.5	118	TP[14]	-8749.95	-362.5
5	SYNC_R[4]	-13706.00	94	62	VGH	-11269.21	-362.5	119	TP[15]	-8704.96	-362.5
6	SYNC_R[5]	-13606.03	54	63	VGH	-11224.22	-362.5	120	TP[16]	-8659.97	-362.5
7	SYNC_R[6]	-13706.00	14	64	T_S[1996]	-11179.24	-362.5	121	TP[17]	-8614.99	-362.5
8	SYNC_R[7]	-13606.03	-26	65	T_S[1995]	-11134.25	-362.5	122	CAS	-8570.00	-362.5
9	SYNC_R[8]	-13706.00	-66	66	VGH_REG	-11089.26	-362.5	123	VSS	-8525.01	-362.5
10	DUMMY[1]	-13618.53	-362.5	67	VGH_REG	-11044.28	-362.5	124	SDLOC	-8480.03	-362.5
11	GOUTR[1]	-13573.54	-362.5	68	VGH_REG	-10999.29	-362.5	125	SDLOC	-8435.04	-362.5
12	GOUTR[2]	-13528.55	-362.5	69	VGH_REG	-10954.30	-362.5	126	ZIGZAG	-8390.05	-362.5
13	GOUTR[3]	-13483.56	-362.5	70	VGH_REG	-10909.32	-362.5	127	ZIGZAG	-8345.06	-362.5
14	GOUTR[4]	-13438.58	-362.5	71	VSN	-10864.33	-362.5	128	ZTYPE	-8300.08	-362.5
15	GOUTR[5]	-13393.59	-362.5	72	VSN	-10819.34	-362.5	129	ZTYPE	-8255.09	-362.5
16	GOUTR[6]	-13348.60	-362.5	73	VSN	-10774.36	-362.5	130	TP[18]	-8210.10	-362.5
17	GOUTR[7]	-13303.62	-362.5	74	VSN	-10729.37	-362.5	131	TP[19]	-8165.12	-362.5
18	GOUTR[8]	-13258.63	-362.5	75	VSN	-10684.38	-362.5	132	TP[20]	-8120.13	-362.5
19	GOUTR[9]	-13213.64	-362.5	76	VSN	-10639.39	-362.5	133	TP[21]	-8075.14	-362.5
20	GOUTR[10]	-13168.66	-362.5	77	VSN	-10594.41	-362.5	134	TP[22]	-8030.16	-362.5
21	GOUTR[11]	-13123.67	-362.5	78	VSP	-10549.42	-362.5	135	TP[23]	-7985.17	-362.5
22	GOUTR[12]	-13078.68	-362.5	79	VSP	-10504.43	-362.5	136	TP[24]	-7940.18	-362.5
23	GOUTR[13]	-13033.70	-362.5	80	VSP	-10459.45	-362.5	137	TP[25]	-7895.20	-362.5
24	GOUTR[14]	-12988.71	-362.5	81	VSP	-10414.46	-362.5	138	TP[26]	-7850.21	-362.5
25	GOUTR[15]	-12943.72	-362.5	82	VSP	-10369.47	-362.5	139	TP[27]	-7805.22	-362.5
26	GOUTR[16]	-12898.74	-362.5	83	VSP	-10324.49	-362.5	140	TP[28]	-7760.24	-362.5
27	GOUTR[17]	-12853.75	-362.5	84	VSP	-10279.50	-362.5	141	TP[29]	-7715.25	-362.5
28	GOUTR[18]	-12808.76	-362.5	85	VSSA	-10234.51	-362.5	142	TP[30]	-7670.26	-362.5
29	GOUTR[19]	-12763.77	-362.5	86	VSSA	-10189.53	-362.5	143	TP[31]	-7625.27	-362.5
30	GOUTR[20]	-12718.79	-362.5	87	VSSA	-10144.54	-362.5	144	TP[32]	-7580.29	-362.5
31	GOUTR[21]	-12673.80	-362.5	88	VSSA	-10099.55	-362.5	145	TP[33]	-7535.30	-362.5
32	GOUTR[22]	-12628.81	-362.5	89	VSSA	-10054.57	-362.5	146	TP[34]	-7490.31	-362.5
33	PASS1_R	-12583.83	-362.5	90	VSSA	-10009.58	-362.5	147	TP[35]	-7445.33	-362.5
34	PASS1_R	-12538.84	-362.5	91	VSSA	-9964.59	-362.5	148	TP[36]	-7400.34	-362.5
35	PASS1_R	-12493.85	-362.5	92	VSSA	-9919.61	-362.5	149	TP[37]	-7355.35	-362.5
36	VCOM	-12438.87	-362.5	93	VSS	-9874.62	-362.5	150	TP[38]	-7310.37	-362.5
37	VCOM	-12393.88	-362.5	94	VSS	-9829.63	-362.5	151	TP[39]	-7265.38	-362.5
38	VCOM	-12348.90	-362.5	95	VSS	-9784.64	-362.5	152	TP[40]	-7220.39	-362.5
39	VCOM	-12303.91	-362.5	96	VSS	-9739.66	-362.5	153	TP[41]	-7175.41	-362.5
40	PASS2_R	-12258.92	-362.5	97	VSS	-9694.67	-362.5	154	TP[42]	-7130.42	-362.5
41	PASS2_R	-12213.94	-362.5	98	VSS	-9649.68	-362.5	155	RESETB	-7085.43	-362.5
42	PASS2_R	-12168.95	-362.5	99	VSS	-9604.70	-362.5	156	RESETB	-7040.45	-362.5
43	VGL	-12123.96	-362.5	100	VSS	-9559.71	-362.5	157	RESETB	-6995.46	-362.5
44	VGL	-12078.97	-362.5	101	VDD_18V	-9514.72	-362.5	158	RESETB	-6950.47	-362.5
45	VGL	-12033.99	-362.5	102	VDD_18V	-9469.74	-362.5	159	LNSW[1]	-6905.48	-362.5
46	VGL	-11989.00	-362.5	103	VDD_18V	-9424.75	-362.5	160	LNSW[1]	-6860.50	-362.5
47	VGL	-11944.01	-362.5	104	TP[0]	-9379.76	-362.5	161	LNSW[0]	-6815.51	-362.5
48	VGL	-11899.03	-362.5	105	TP[1]	-9334.78	-362.5	162	LNSW[0]	-6770.52	-362.5
49	VGL	-11854.04	-362.5	106	TP[2]	-9289.79	-362.5	163	PNSW	-6725.54	-362.5
50	VGL_REG	-11809.05	-362.5	107	TP[3]	-9244.80	-362.5	164	PNSW	-6680.55	-362.5
51	VGL_REG	-11764.07	-362.5	108	TP[4]	-9199.82	-362.5	165	IFSEL[1]	-6635.56	-362.5
52	VGL_REG	-11719.08	-362.5	109	TP[5]	-9154.83	-362.5	166	IFSEL[1]	-6590.58	-362.5
53	VGL_REG	-11674.09	-362.5	110	TP[6]	-9109.84	-362.5	167	IFSEL[0]	-6545.59	-362.5
54	VGL_REG	-11629.11	-362.5	111	TP[7]	-9064.85	-362.5	168	IFSEL[0]	-6500.60	-362.5
55	VGL_REG	-11584.12	-362.5	112	TP[8]	-9019.87	-362.5	169	RES[2]	-6455.62	-362.5
56	VGL_REG	-11539.13	-362.5	113	TP[9]	-8974.88	-362.5	170	VSS	-6410.63	-362.5
57	VGH	-11494.15	-362.5	114	TP[10]	-8929.89	-362.5	171	RES[1]	-6365.64	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
172	VSS	-6320.66	-362.5	229	VDDIO	-3756.40	-362.5	286	VSS_IF	-1192.15	-362.5
173	RES[0]	-6275.67	-362.5	230	VDD	-3711.42	-362.5	287	VSS_IF	-1147.17	-362.5
174	VSS	-6230.68	-362.5	231	VDD	-3666.43	-362.5	288	VSS_IF	-1102.18	-362.5
175	GATE_SW[1]	-6185.69	-362.5	232	VDD	-3621.44	-362.5	289	VSS_IF	-1057.19	-362.5
176	GATE_SW[1]	-6140.71	-362.5	233	VDD	-3576.46	-362.5	290	DP[0]	-1012.20	-362.5
177	GATE_SW[0]	-6095.72	-362.5	234	VDD	-3531.47	-362.5	291	DP[0]	-967.22	-362.5
178	GATE_SW[0]	-6050.73	-362.5	235	VDD	-3486.48	-362.5	292	DP[0]	-922.23	-362.5
179	OP_DRV[1]	-6005.75	-362.5	236	VCL	-3441.50	-362.5	293	DP[0]	-877.24	-362.5
180	OP_DRV[1]	-5960.76	-362.5	237	VCL	-3396.51	-362.5	294	DP[0]	-832.26	-362.5
181	OP_DRV[0]	-5915.77	-362.5	238	VCL	-3351.52	-362.5	295	DP[0]	-787.27	-362.5
182	OP_DRV[0]	-5870.79	-362.5	239	VCL	-3306.54	-362.5	296	DN[0]	-742.28	-362.5
183	GIP_LRSEL[1]	-5825.80	-362.5	240	VCL	-3261.55	-362.5	297	DN[0]	-697.30	-362.5
184	VSS	-5780.81	-362.5	241	VSN	-3216.56	-362.5	298	DN[0]	-652.31	-362.5
185	GIP_LRSEL[0]	-5735.83	-362.5	242	VSN	-3171.57	-362.5	299	DN[0]	-607.32	-362.5
186	VSS	-5690.84	-362.5	243	VSN	-3126.59	-362.5	300	DN[0]	-562.34	-362.5
187	DVCOM_EN	-5645.85	-362.5	244	VSN	-3081.60	-362.5	301	DN[0]	-517.35	-362.5
188	DVCOM_EN	-5600.87	-362.5	245	VSN	-3036.61	-362.5	302	VSS_IF	-472.36	-362.5
189	DITHER_EN	-5555.88	-362.5	246	VSN	-2991.63	-362.5	303	DP[1]	-427.38	-362.5
190	DITHER_EN	-5510.89	-362.5	247	VSN	-2946.64	-362.5	304	DP[1]	-382.39	-362.5
191	HFRC_EN	-5465.90	-362.5	248	VSN	-2901.65	-362.5	305	DP[1]	-337.40	-362.5
192	HFRC_EN	-5420.92	-362.5	249	VSP	-2856.67	-362.5	306	DP[1]	-292.41	-362.5
193	STBYB	-5375.93	-362.5	250	VSP	-2811.68	-362.5	307	DP[1]	-247.43	-362.5
194	STBYB	-5330.94	-362.5	251	VSP	-2766.69	-362.5	308	DP[1]	-202.44	-362.5
195	BISTB	-5285.96	-362.5	252	VSP	-2721.71	-362.5	309	DN[1]	-157.45	-362.5
196	BISTB	-5240.97	-362.5	253	VSP	-2676.72	-362.5	310	DN[1]	-112.47	-362.5
197	CMD_SEL	-5195.98	-362.5	254	VSP	-2631.73	-362.5	311	DN[1]	-67.48	-362.5
198	CMD_SEL	-5151.00	-362.5	255	VSP	-2586.75	-362.5	312	DN[1]	-22.49	-362.5
199	LVFMT	-5106.01	-362.5	256	VSSA	-2541.76	-362.5	313	DN[1]	22.49	-362.5
200	LVFMT	-5061.02	-362.5	257	VSSA	-2496.77	-362.5	314	DN[1]	67.48	-362.5
201	LVBIT	-5016.04	-362.5	258	VSSA	-2451.78	-362.5	315	VSS_IF	112.47	-362.5
202	LVBIT	-4971.05	-362.5	259	VSSA	-2406.80	-362.5	316	CKP	157.45	-362.5
203	SDA	-4926.06	-362.5	260	VSSA	-2361.81	-362.5	317	CKP	202.44	-362.5
204	SDA	-4881.08	-362.5	261	VSSA	-2316.82	-362.5	318	CKP	247.43	-362.5
205	SCL	-4836.09	-362.5	262	VSSA	-2271.84	-362.5	319	CKP	292.41	-362.5
206	SCL	-4791.10	-362.5	263	VGMP	-2226.85	-362.5	320	CKP	337.40	-362.5
207	CSB	-4746.11	-362.5	264	VGMP	-2181.86	-362.5	321	CKP	382.39	-362.5
208	CSB	-4701.13	-362.5	265	VGMP	-2136.88	-362.5	322	CKN	427.38	-362.5
209	FRAME	-4656.14	-362.5	266	VGMP	-2091.89	-362.5	323	CKN	472.36	-362.5
210	FRAME	-4611.15	-362.5	267	VGMP	-2046.90	-362.5	324	CKN	517.35	-362.5
211	DUMMY[2]	-4566.17	-362.5	268	VGMP	-2001.92	-362.5	325	CKN	562.34	-362.5
212	T_VTSEN[2]	-4521.18	-362.5	269	VGMN	-1956.93	-362.5	326	CKN	607.32	-362.5
213	T_VTSEN[1]	-4476.19	-362.5	270	VGMN	-1911.94	-362.5	327	CKN	652.31	-362.5
214	T_VTSEN[0]	-4431.21	-362.5	271	VGMN	-1866.96	-362.5	328	VSS_IF	697.30	-362.5
215	LEDON	-4386.22	-362.5	272	VGMN	-1821.97	-362.5	329	DP[2]	742.28	-362.5
216	LEDON	-4341.23	-362.5	273	VGMN	-1776.98	-362.5	330	DP[2]	787.27	-362.5
217	LEDPWM	-4296.25	-362.5	274	VGMN	-1731.99	-362.5	331	DP[2]	832.26	-362.5
218	LEDPWM	-4251.26	-362.5	275	DUMMY[4]	-1687.01	-362.5	332	DP[2]	877.24	-362.5
219	PWR_EN	-4206.27	-362.5	276	DUMMY[5]	-1642.02	-362.5	333	DP[2]	922.23	-362.5
220	PWR_EN	-4161.29	-362.5	277	DUMMY[6]	-1597.03	-362.5	334	DP[2]	967.22	-362.5
221	DUMMY[3]	-4116.30	-362.5	278	DUMMY[7]	-1552.05	-362.5	335	DN[2]	1012.20	-362.5
222	TP[43]	-4071.31	-362.5	279	DUMMY[8]	-1507.06	-362.5	336	DN[2]	1057.19	-362.5
223	TP[44]	-4026.32	-362.5	280	DUMMY[9]	-1462.07	-362.5	337	DN[2]	1102.18	-362.5
224	VDDIO	-3981.34	-362.5	281	DUMMY[10]	-1417.09	-362.5	338	DN[2]	1147.17	-362.5
225	VDDIO	-3936.35	-362.5	282	VSS_IF	-1372.10	-362.5	339	DN[2]	1192.15	-362.5
226	VDDIO	-3891.36	-362.5	283	VSS_IF	-1327.11	-362.5	340	DN[2]	1237.14	-362.5
227	VDDIO	-3846.38	-362.5	284	VSS_IF	-1282.13	-362.5	341	VSS_IF	1282.13	-362.5
228	VDDIO	-3801.39	-362.5	285	VSS_IF	-1237.14	-362.5	342	DP[3]	1327.11	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
343	DP[3]	1372.10	-362.5	400	VDD_18V	3936.35	-362.5	457	TP[55]	6500.60	-362.5
344	DP[3]	1417.09	-362.5	401	VDD_18V	3981.34	-362.5	458	TP[56]	6545.59	-362.5
345	DP[3]	1462.07	-362.5	402	VDD_18V	4026.32	-362.5	459	TP[57]	6590.58	-362.5
346	DP[3]	1507.06	-362.5	403	VDD_18V	4071.31	-362.5	460	TP[58]	6635.56	-362.5
347	DP[3]	1552.05	-362.5	404	VDD_18V	4116.30	-362.5	461	TP[59]	6680.55	-362.5
348	DN[3]	1597.03	-362.5	405	VDD_18V	4161.29	-362.5	462	TP[60]	6725.54	-362.5
349	DN[3]	1642.02	-362.5	406	VDD_18V	4206.27	-362.5	463	TP[61]	6770.52	-362.5
350	DN[3]	1687.01	-362.5	407	VDD_18V	4251.26	-362.5	464	TP[62]	6815.51	-362.5
351	DN[3]	1731.99	-362.5	408	VDD_18V	4296.25	-362.5	465	TP[63]	6860.50	-362.5
352	DN[3]	1776.98	-362.5	409	VDD_18V	4341.23	-362.5	466	TP[64]	6905.48	-362.5
353	DN[3]	1821.97	-362.5	410	VDD_18V	4386.22	-362.5	467	TP[65]	6950.47	-362.5
354	VSS_IF	1866.96	-362.5	411	VDD	4431.21	-362.5	468	TP[66]	6995.46	-362.5
355	VSS_IF	1911.94	-362.5	412	VDD	4476.19	-362.5	469	TP[67]	7040.45	-362.5
356	DUMMY[11]	1956.93	-362.5	413	VDD	4521.18	-362.5	470	TP[68]	7085.43	-362.5
357	DUMMY[12]	2001.92	-362.5	414	VDD	4566.17	-362.5	471	TP[69]	7130.42	-362.5
358	TP[45]	2046.90	-362.5	415	VDD	4611.15	-362.5	472	TP[70]	7175.41	-362.5
359	TP[46]	2091.89	-362.5	416	VDD	4656.14	-362.5	473	CS_GIP	7220.39	-362.5
360	TP[47]	2136.88	-362.5	417	VDD	4701.13	-362.5	474	CS_GIP	7265.38	-362.5
361	TP[48]	2181.86	-362.5	418	VDD	4746.11	-362.5	475	CS_SD	7310.37	-362.5
362	TP[49]	2226.85	-362.5	419	VDD	4791.10	-362.5	476	CS_SD	7355.35	-362.5
363	TP[50]	2271.84	-362.5	420	VDD	4836.09	-362.5	477	DIR	7400.34	-362.5
364	VSS	2316.82	-362.5	421	VDD_IF	4881.08	-362.5	478	DIR	7445.33	-362.5
365	VSS	2361.81	-362.5	422	VDD_IF	4926.06	-362.5	479	REV	7490.31	-362.5
366	VSS	2406.80	-362.5	423	VDD_IF	4971.05	-362.5	480	REV	7535.30	-362.5
367	VSS	2451.78	-362.5	424	VDD_IF	5016.04	-362.5	481	H2DOT	7580.29	-362.5
368	VSS	2496.77	-362.5	425	VDD_IF	5061.02	-362.5	482	H2DOT	7625.27	-362.5
369	VSS	2541.76	-362.5	426	VDD_IF	5106.01	-362.5	483	POLC	7670.26	-362.5
370	VSS	2586.75	-362.5	427	VDD_IF	5151.00	-362.5	484	POLC	7715.25	-362.5
371	VSS	2631.73	-362.5	428	VDD_IF	5195.98	-362.5	485	A0	7760.24	-362.5
372	VSS	2676.72	-362.5	429	VDD_IF	5240.97	-362.5	486	A0	7805.22	-362.5
373	VSS	2721.71	-362.5	430	VDD_IF	5285.96	-362.5	487	DVCOM_WP	7850.21	-362.5
374	VSS	2766.69	-362.5	431	VDDIO	5330.94	-362.5	488	DVCOM_WP	7895.20	-362.5
375	VSS	2811.68	-362.5	432	VDDIO	5375.93	-362.5	489	SCL_I2C	7940.18	-362.5
376	VGH_REG	2856.67	-362.5	433	VDDIO	5420.92	-362.5	490	SCL_I2C	7985.17	-362.5
377	VGH_REG	2901.65	-362.5	434	VDDIO	5465.90	-362.5	491	SDA_I2C	8030.16	-362.5
378	VGH_REG	2946.64	-362.5	435	VDDIO	5510.89	-362.5	492	SDA_I2C	8075.14	-362.5
379	VGH_REG	2991.63	-362.5	436	VDDIO	5555.88	-362.5	493	SCAN_SEL	8120.13	-362.5
380	DUMMY[13]	3036.61	-362.5	437	VDDIO	5600.87	-362.5	494	SCAN_SEL	8165.12	-362.5
381	DUMMY[14]	3081.60	-362.5	438	VDDIO	5645.85	-362.5	495	INV_SEL[1]	8210.10	-362.5
382	DUMMY[15]	3126.59	-362.5	439	VDDIO	5690.84	-362.5	496	INV_SEL[1]	8255.09	-362.5
383	DUMMY[16]	3171.57	-362.5	440	VDDIO	5735.83	-362.5	497	INV_SEL[0]	8300.08	-362.5
384	DUMMY[17]	3216.56	-362.5	441	DUMMY[20]	5780.81	-362.5	498	INV_SEL[0]	8345.06	-362.5
385	DUMMY[18]	3261.55	-362.5	442	DUMMY[21]	5825.80	-362.5	499	DUMMY[30]	8390.05	-362.5
386	DUMMY[19]	3306.54	-362.5	443	DUMMY[22]	5870.79	-362.5	500	TP[71]	8435.04	-362.5
387	VDD_18V_IF	3351.52	-362.5	444	DUMMY[23]	5915.77	-362.5	501	TP[72]	8480.03	-362.5
388	VDD_18V_IF	3396.51	-362.5	445	DUMMY[24]	5960.76	-362.5	502	TP[73]	8525.01	-362.5
389	VDD_18V_IF	3441.50	-362.5	446	DUMMY[25]	6005.75	-362.5	503	DUMMY[31]	8570.00	-362.5
390	VDD_18V_IF	3486.48	-362.5	447	DUMMY[26]	6050.73	-362.5	504	DUMMY[32]	8614.99	-362.5
391	VDD_18V_IF	3531.47	-362.5	448	DUMMY[27]	6095.72	-362.5	505	DUMMY[33]	8659.97	-362.5
392	VDD_18V_IF	3576.46	-362.5	449	DUMMY[28]	6140.71	-362.5	506	DUMMY[34]	8704.96	-362.5
393	VDD_18V_IF	3621.44	-362.5	450	DUMMY[29]	6185.69	-362.5	507	DUMMY[35]	8749.95	-362.5
394	VDD_18V_IF	3666.43	-362.5	451	TP[51]	6230.68	-362.5	508	VSN	8794.93	-362.5
395	VDD_18V_IF	3711.42	-362.5	452	TP[52]	6275.67	-362.5	509	VSN	8839.92	-362.5
396	VDD_18V_IF	3756.40	-362.5	453	UPDN	6320.66	-362.5	510	VSN	8884.91	-362.5
397	VDD_18V_IF	3801.39	-362.5	454	UPDN	6365.64	-362.5	511	VSN	8929.89	-362.5
398	VDD_18V_IF	3846.38	-362.5	455	TP[53]	6410.63	-362.5	512	VSN	8974.88	-362.5
399	VDD_18V	3891.36	-362.5	456	TP[54]	6455.62	-362.5	513	VSN	9019.87	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
514	VSN	9064.85	-362.5	571	VGL_REG	11629.11	-362.5	628	DUMMY[40]	13400.09	192.5
515	VSP	9109.84	-362.5	572	VGL_REG	11674.09	-362.5	629	DUMMY[41]	13388.09	282.5
516	VSP	9154.83	-362.5	573	VGL	11719.08	-362.5	630	DUMMY[42]	13376.10	372.5
517	VSP	9199.82	-362.5	574	VGL	11764.07	-362.5	631	PASS1_L	13364.10	192.5
518	VSP	9244.80	-362.5	575	VGL	11809.05	-362.5	632	PASS1_L	13352.10	282.5
519	VSP	9289.79	-362.5	576	VGL	11854.04	-362.5	633	PASS1_L	13340.11	372.5
520	VSP	9334.78	-362.5	577	VGL	11899.03	-362.5	634	PASS1_L	13328.11	192.5
521	VSP	9379.76	-362.5	578	VGL	11944.01	-362.5	635	PASS1_L	13316.11	282.5
522	VSSA	9424.75	-362.5	579	VGL	11989.00	-362.5	636	PASS1_L	13304.12	372.5
523	VSSA	9469.74	-362.5	580	VGL	12033.99	-362.5	637	VCOM	13292.12	192.5
524	VSSA	9514.72	-362.5	581	VGL	12078.97	-362.5	638	VCOM	13280.12	282.5
525	VSSA	9559.71	-362.5	582	VGL	12123.96	-362.5	639	VCOM	13268.13	372.5
526	VSSA	9604.70	-362.5	583	PASS2_L	12168.95	-362.5	640	VCOM	13256.13	192.5
527	VSSA	9649.68	-362.5	584	PASS2_L	12213.94	-362.5	641	VCOM	13244.13	282.5
528	VSSA	9694.67	-362.5	585	PASS2_L	12258.92	-362.5	642	VCOM	13232.14	372.5
529	VSSA	9739.66	-362.5	586	VCOM	12303.91	-362.5	643	PASS2_L	13220.14	192.5
530	VSS	9784.64	-362.5	587	VCOM	12348.90	-362.5	644	PASS2_L	13208.15	282.5
531	VSS	9829.63	-362.5	588	VCOM	12393.88	-362.5	645	PASS2_L	13196.15	372.5
532	VSS	9874.62	-362.5	589	VCOM	12438.87	-362.5	646	PASS2_L	13184.15	192.5
533	VSS	9919.61	-362.5	590	PASS1_L	12493.85	-362.5	647	PASS2_L	13172.16	282.5
534	VSS	9964.59	-362.5	591	PASS1_L	12538.84	-362.5	648	PASS2_L	13160.16	372.5
535	VSS	10009.58	-362.5	592	PASS1_L	12583.83	-362.5	649	DUMMY[43]	13148.16	192.5
536	VSS	10054.57	-362.5	593	GOUTL[22]	12628.81	-362.5	650	DUMMY[44]	13136.17	282.5
537	VDD_18V	10099.55	-362.5	594	GOUTL[21]	12673.80	-362.5	651	DUMMY[45]	13124.17	372.5
538	VDD_18V	10144.54	-362.5	595	GOUTL[20]	12718.79	-362.5	652	DUMMY[46]	13112.17	192.5
539	VDD_18V	10189.53	-362.5	596	GOUTL[19]	12763.77	-362.5	653	DUMMY[47]	13100.18	282.5
540	VDD_18V	10234.51	-362.5	597	GOUTL[18]	12808.76	-362.5	654	DUMMY[48]	13088.18	372.5
541	VDD_18V	10279.50	-362.5	598	GOUTL[17]	12853.75	-362.5	655	S[0]	13076.18	192.5
542	VDD_18V	10324.49	-362.5	599	GOUTL[16]	12898.74	-362.5	656	S[1]	13064.19	282.5
543	VGH_REG	10369.47	-362.5	600	GOUTL[15]	12943.72	-362.5	657	S[2]	13052.19	372.5
544	VGH_REG	10414.46	-362.5	601	GOUTL[14]	12988.71	-362.5	658	S[3]	13040.19	192.5
545	VGH_REG	10459.45	-362.5	602	GOUTL[13]	13033.70	-362.5	659	S[4]	13028.20	282.5
546	VGH_REG	10504.43	-362.5	603	GOUTL[12]	13078.68	-362.5	660	S[5]	13016.20	372.5
547	VGH_REG	10549.42	-362.5	604	GOUTL[11]	13123.67	-362.5	661	S[6]	13004.20	192.5
548	VGH_REG	10594.41	-362.5	605	GOUTL[10]	13168.66	-362.5	662	S[7]	12992.21	282.5
549	VGH_REG	10639.39	-362.5	606	GOUTL[9]	13213.64	-362.5	663	S[8]	12980.21	372.5
550	VGH_REG	10684.38	-362.5	607	GOUTL[8]	13258.63	-362.5	664	S[9]	12968.22	192.5
551	VGH_REG	10729.37	-362.5	608	GOUTL[7]	13303.62	-362.5	665	S[10]	12956.22	282.5
552	VGH_REG	10774.36	-362.5	609	GOUTL[6]	13348.60	-362.5	666	S[11]	12944.22	372.5
553	T_S[115]	10819.34	-362.5	610	GOUTL[5]	13393.59	-362.5	667	S[12]	12932.23	192.5
554	T_S[114]	10864.33	-362.5	611	GOUTL[4]	13438.58	-362.5	668	S[13]	12920.23	282.5
555	VGH	10909.32	-362.5	612	GOUTL[3]	13483.56	-362.5	669	S[14]	12908.23	372.5
556	VGH	10954.30	-362.5	613	GOUTL[2]	13528.55	-362.5	670	S[15]	12896.24	192.5
557	VGH	10999.29	-362.5	614	GOUTL[1]	13573.54	-362.5	671	S[16]	12884.24	282.5
558	VGH	11044.28	-362.5	615	DUMMY[36]	13618.53	-362.5	672	S[17]	12872.24	372.5
559	VGH	11089.26	-362.5	616	SYNC_L[8]	13706.00	-66	673	S[18]	12860.25	192.5
560	VGH	11134.25	-362.5	617	SYNC_L[7]	13606.03	-26	674	S[19]	12848.25	282.5
561	VGH	11179.24	-362.5	618	SYNC_L[6]	13706.00	14	675	S[20]	12836.25	372.5
562	VGH	11224.22	-362.5	619	SYNC_L[5]	13606.03	54	676	S[21]	12824.26	192.5
563	VGH	11269.21	-362.5	620	SYNC_L[4]	13706.00	94	677	S[22]	12812.26	282.5
564	VGH	11314.20	-362.5	621	SYNC_L[3]	13606.03	134	678	S[23]	12800.26	372.5
565	VGL_REG	11359.18	-362.5	622	SYNC_L[2]	13706.00	174	679	S[24]	12788.27	192.5
566	VGL_REG	11404.17	-362.5	623	SYNC_L[1]	13606.03	214	680	S[25]	12776.27	282.5
567	VGL_REG	11449.16	-362.5	624	SYNC_L[0]	13706.00	254	681	S[26]	12764.27	372.5
568	VGL_REG	11494.15	-362.5	625	DUMMY[37]	13436.08	192.5	682	S[27]	12752.28	192.5
569	VGL_REG	11539.13	-362.5	626	DUMMY[38]	13424.08	282.5	683	S[28]	12740.28	282.5
570	VGL_REG	11584.12	-362.5	627	DUMMY[39]	13412.09	372.5	684	S[29]	12728.29	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
685	S[30]	12716.29	192.5	742	S[87]	12032.49	192.5	799	S[144]	11348.69	192.5
686	S[31]	12704.29	282.5	743	S[88]	12020.49	282.5	800	S[145]	11336.69	282.5
687	S[32]	12692.30	372.5	744	S[89]	12008.50	372.5	801	S[146]	11324.69	372.5
688	S[33]	12680.30	192.5	745	S[90]	11996.50	192.5	802	S[147]	11312.70	192.5
689	S[34]	12668.30	282.5	746	S[91]	11984.50	282.5	803	S[148]	11300.70	282.5
690	S[35]	12656.31	372.5	747	S[92]	11972.51	372.5	804	S[149]	11288.71	372.5
691	S[36]	12644.31	192.5	748	S[93]	11960.51	192.5	805	S[150]	11276.71	192.5
692	S[37]	12632.31	282.5	749	S[94]	11948.51	282.5	806	S[151]	11264.71	282.5
693	S[38]	12620.32	372.5	750	S[95]	11936.52	372.5	807	S[152]	11252.72	372.5
694	S[39]	12608.32	192.5	751	S[96]	11924.52	192.5	808	S[153]	11240.72	192.5
695	S[40]	12596.32	282.5	752	S[97]	11912.52	282.5	809	S[154]	11228.72	282.5
696	S[41]	12584.33	372.5	753	S[98]	11900.53	372.5	810	S[155]	11216.73	372.5
697	S[42]	12572.33	192.5	754	S[99]	11888.53	192.5	811	S[156]	11204.73	192.5
698	S[43]	12560.33	282.5	755	S[100]	11876.53	282.5	812	S[157]	11192.73	282.5
699	S[44]	12548.34	372.5	756	S[101]	11864.54	372.5	813	S[158]	11180.74	372.5
700	S[45]	12536.34	192.5	757	S[102]	11852.54	192.5	814	S[159]	11168.74	192.5
701	S[46]	12524.34	282.5	758	S[103]	11840.54	282.5	815	S[160]	11156.74	282.5
702	S[47]	12512.35	372.5	759	S[104]	11828.55	372.5	816	S[161]	11144.75	372.5
703	S[48]	12500.35	192.5	760	S[105]	11816.55	192.5	817	S[162]	11132.75	192.5
704	S[49]	12488.36	282.5	761	S[106]	11804.55	282.5	818	S[163]	11120.75	282.5
705	S[50]	12476.36	372.5	762	S[107]	11792.56	372.5	819	S[164]	11108.76	372.5
706	S[51]	12464.36	192.5	763	S[108]	11780.56	192.5	820	S[165]	11096.76	192.5
707	S[52]	12452.37	282.5	764	S[109]	11768.57	282.5	821	S[166]	11084.76	282.5
708	S[53]	12440.37	372.5	765	S[110]	11756.57	372.5	822	S[167]	11072.77	372.5
709	S[54]	12428.37	192.5	766	S[111]	11744.57	192.5	823	S[168]	11060.77	192.5
710	S[55]	12416.38	282.5	767	S[112]	11732.58	282.5	824	S[169]	11048.78	282.5
711	S[56]	12404.38	372.5	768	S[113]	11720.58	372.5	825	S[170]	11036.78	372.5
712	S[57]	12392.38	192.5	769	S[114]	11708.58	192.5	826	S[171]	11024.78	192.5
713	S[58]	12380.39	282.5	770	S[115]	11696.59	282.5	827	S[172]	11012.79	282.5
714	S[59]	12368.39	372.5	771	S[116]	11684.59	372.5	828	S[173]	11000.79	372.5
715	S[60]	12356.39	192.5	772	S[117]	11672.59	192.5	829	S[174]	10988.79	192.5
716	S[61]	12344.40	282.5	773	S[118]	11660.60	282.5	830	S[175]	10976.80	282.5
717	S[62]	12332.40	372.5	774	S[119]	11648.60	372.5	831	S[176]	10964.80	372.5
718	S[63]	12320.40	192.5	775	S[120]	11636.60	192.5	832	S[177]	10952.80	192.5
719	S[64]	12308.41	282.5	776	S[121]	11624.61	282.5	833	S[178]	10940.81	282.5
720	S[65]	12296.41	372.5	777	S[122]	11612.61	372.5	834	S[179]	10928.81	372.5
721	S[66]	12284.41	192.5	778	S[123]	11600.61	192.5	835	S[180]	10916.81	192.5
722	S[67]	12272.42	282.5	779	S[124]	11588.62	282.5	836	S[181]	10904.82	282.5
723	S[68]	12260.42	372.5	780	S[125]	11576.62	372.5	837	S[182]	10892.82	372.5
724	S[69]	12248.43	192.5	781	S[126]	11564.62	192.5	838	S[183]	10880.82	192.5
725	S[70]	12236.43	282.5	782	S[127]	11552.63	282.5	839	S[184]	10868.83	282.5
726	S[71]	12224.43	372.5	783	S[128]	11540.63	372.5	840	S[185]	10856.83	372.5
727	S[72]	12212.44	192.5	784	S[129]	11528.64	192.5	841	S[186]	10844.84	192.5
728	S[73]	12200.44	282.5	785	S[130]	11516.64	282.5	842	S[187]	10832.84	282.5
729	S[74]	12188.44	372.5	786	S[131]	11504.64	372.5	843	S[188]	10820.84	372.5
730	S[75]	12176.45	192.5	787	S[132]	11492.65	192.5	844	S[189]	10808.85	192.5
731	S[76]	12164.45	282.5	788	S[133]	11480.65	282.5	845	S[190]	10796.85	282.5
732	S[77]	12152.45	372.5	789	S[134]	11468.65	372.5	846	S[191]	10784.85	372.5
733	S[78]	12140.46	192.5	790	S[135]	11456.66	192.5	847	S[192]	10772.86	192.5
734	S[79]	12128.46	282.5	791	S[136]	11444.66	282.5	848	S[193]	10760.86	282.5
735	S[80]	12116.46	372.5	792	S[137]	11432.66	372.5	849	S[194]	10748.86	372.5
736	S[81]	12104.47	192.5	793	S[138]	11420.67	192.5	850	S[195]	10736.87	192.5
737	S[82]	12092.47	282.5	794	S[139]	11408.67	282.5	851	S[196]	10724.87	282.5
738	S[83]	12080.47	372.5	795	S[140]	11396.67	372.5	852	S[197]	10712.87	372.5
739	S[84]	12068.48	192.5	796	S[141]	11384.68	192.5	853	S[198]	10700.88	192.5
740	S[85]	12056.48	282.5	797	S[142]	11372.68	282.5	854	S[199]	10688.88	282.5
741	S[86]	12044.48	372.5	798	S[143]	11360.68	372.5	855	S[200]	10676.88	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
856	S[201]	10664.89	192.5	913	S[258]	9981.09	192.5	970	S[315]	9297.29	192.5
857	S[202]	10652.89	282.5	914	S[259]	9969.09	282.5	971	S[316]	9285.29	282.5
858	S[203]	10640.89	372.5	915	S[260]	9957.09	372.5	972	S[317]	9273.29	372.5
859	S[204]	10628.90	192.5	916	S[261]	9945.10	192.5	973	S[318]	9261.30	192.5
860	S[205]	10616.90	282.5	917	S[262]	9933.10	282.5	974	S[319]	9249.30	282.5
861	S[206]	10604.91	372.5	918	S[263]	9921.10	372.5	975	S[320]	9237.30	372.5
862	S[207]	10592.91	192.5	919	S[264]	9909.11	192.5	976	S[321]	9225.31	192.5
863	S[208]	10580.91	282.5	920	S[265]	9897.11	282.5	977	S[322]	9213.31	282.5
864	S[209]	10568.92	372.5	921	S[266]	9885.12	372.5	978	S[323]	9201.31	372.5
865	S[210]	10556.92	192.5	922	S[267]	9873.12	192.5	979	S[324]	9189.32	192.5
866	S[211]	10544.92	282.5	923	S[268]	9861.12	282.5	980	S[325]	9177.32	282.5
867	S[212]	10532.93	372.5	924	S[269]	9849.13	372.5	981	S[326]	9165.33	372.5
868	S[213]	10520.93	192.5	925	S[270]	9837.13	192.5	982	S[327]	9153.33	192.5
869	S[214]	10508.93	282.5	926	S[271]	9825.13	282.5	983	S[328]	9141.33	282.5
870	S[215]	10496.94	372.5	927	S[272]	9813.14	372.5	984	S[329]	9129.34	372.5
871	S[216]	10484.94	192.5	928	S[273]	9801.14	192.5	985	S[330]	9117.34	192.5
872	S[217]	10472.94	282.5	929	S[274]	9789.14	282.5	986	S[331]	9105.34	282.5
873	S[218]	10460.95	372.5	930	S[275]	9777.15	372.5	987	S[332]	9093.35	372.5
874	S[219]	10448.95	192.5	931	S[276]	9765.15	192.5	988	S[333]	9081.35	192.5
875	S[220]	10436.95	282.5	932	S[277]	9753.15	282.5	989	S[334]	9069.35	282.5
876	S[221]	10424.96	372.5	933	S[278]	9741.16	372.5	990	S[335]	9057.36	372.5
877	S[222]	10412.96	192.5	934	S[279]	9729.16	192.5	991	S[336]	9045.36	192.5
878	S[223]	10400.96	282.5	935	S[280]	9717.16	282.5	992	S[337]	9033.36	282.5
879	S[224]	10388.97	372.5	936	S[281]	9705.17	372.5	993	S[338]	9021.37	372.5
880	S[225]	10376.97	192.5	937	S[282]	9693.17	192.5	994	S[339]	9009.37	192.5
881	S[226]	10364.98	282.5	938	S[283]	9681.17	282.5	995	S[340]	8997.37	282.5
882	S[227]	10352.98	372.5	939	S[284]	9669.18	372.5	996	S[341]	8985.38	372.5
883	S[228]	10340.98	192.5	940	S[285]	9657.18	192.5	997	S[342]	8973.38	192.5
884	S[229]	10328.99	282.5	941	S[286]	9645.19	282.5	998	S[343]	8961.38	282.5
885	S[230]	10316.99	372.5	942	S[287]	9633.19	372.5	999	S[344]	8949.39	372.5
886	S[231]	10304.99	192.5	943	S[288]	9621.19	192.5	1000	S[345]	8937.39	192.5
887	S[232]	10293.00	282.5	944	S[289]	9609.20	282.5	1001	S[346]	8925.40	282.5
888	S[233]	10281.00	372.5	945	S[290]	9597.20	372.5	1002	S[347]	8913.40	372.5
889	S[234]	10269.00	192.5	946	S[291]	9585.20	192.5	1003	S[348]	8901.40	192.5
890	S[235]	10257.01	282.5	947	S[292]	9573.21	282.5	1004	S[349]	8889.41	282.5
891	S[236]	10245.01	372.5	948	S[293]	9561.21	372.5	1005	S[350]	8877.41	372.5
892	S[237]	10233.01	192.5	949	S[294]	9549.21	192.5	1006	S[351]	8865.41	192.5
893	S[238]	10221.02	282.5	950	S[295]	9537.22	282.5	1007	S[352]	8853.42	282.5
894	S[239]	10209.02	372.5	951	S[296]	9525.22	372.5	1008	S[353]	8841.42	372.5
895	S[240]	10197.02	192.5	952	S[297]	9513.22	192.5	1009	S[354]	8829.42	192.5
896	S[241]	10185.03	282.5	953	S[298]	9501.23	282.5	1010	S[355]	8817.43	282.5
897	S[242]	10173.03	372.5	954	S[299]	9489.23	372.5	1011	S[356]	8805.43	372.5
898	S[243]	10161.03	192.5	955	S[300]	9477.23	192.5	1012	S[357]	8793.43	192.5
899	S[244]	10149.04	282.5	956	S[301]	9465.24	282.5	1013	S[358]	8781.44	282.5
900	S[245]	10137.04	372.5	957	S[302]	9453.24	372.5	1014	S[359]	8769.44	372.5
901	S[246]	10125.05	192.5	958	S[303]	9441.24	192.5	1015	S[360]	8757.44	192.5
902	S[247]	10113.05	282.5	959	S[304]	9429.25	282.5	1016	S[361]	8745.45	282.5
903	S[248]	10101.05	372.5	960	S[305]	9417.25	372.5	1017	S[362]	8733.45	372.5
904	S[249]	10089.06	192.5	961	S[306]	9405.26	192.5	1018	S[363]	8721.45	192.5
905	S[250]	10077.06	282.5	962	S[307]	9393.26	282.5	1019	S[364]	8709.46	282.5
906	S[251]	10065.06	372.5	963	S[308]	9381.26	372.5	1020	S[365]	8697.46	372.5
907	S[252]	10053.07	192.5	964	S[309]	9369.27	192.5	1021	S[366]	8685.47	192.5
908	S[253]	10041.07	282.5	965	S[310]	9357.27	282.5	1022	S[367]	8673.47	282.5
909	S[254]	10029.07	372.5	966	S[311]	9345.27	372.5	1023	S[368]	8661.47	372.5
910	S[255]	10017.08	192.5	967	S[312]	9333.28	192.5	1024	S[369]	8649.48	192.5
911	S[256]	10005.08	282.5	968	S[313]	9321.28	282.5	1025	S[370]	8637.48	282.5
912	S[257]	9993.08	372.5	969	S[314]	9309.28	372.5	1026	S[371]	8625.48	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1027	S[372]	8613.49	192.5	1084	S[429]	7929.69	192.5	1141	S[486]	7245.89	192.5
1028	S[373]	8601.49	282.5	1085	S[430]	7917.69	282.5	1142	S[487]	7233.89	282.5
1029	S[374]	8589.49	372.5	1086	S[431]	7905.69	372.5	1143	S[488]	7221.89	372.5
1030	S[375]	8577.50	192.5	1087	S[432]	7893.70	192.5	1144	S[489]	7209.90	192.5
1031	S[376]	8565.50	282.5	1088	S[433]	7881.70	282.5	1145	S[490]	7197.90	282.5
1032	S[377]	8553.50	372.5	1089	S[434]	7869.70	372.5	1146	S[491]	7185.90	372.5
1033	S[378]	8541.51	192.5	1090	S[435]	7857.71	192.5	1147	S[492]	7173.91	192.5
1034	S[379]	8529.51	282.5	1091	S[436]	7845.71	282.5	1148	S[493]	7161.91	282.5
1035	S[380]	8517.51	372.5	1092	S[437]	7833.71	372.5	1149	S[494]	7149.91	372.5
1036	S[381]	8505.52	192.5	1093	S[438]	7821.72	192.5	1150	S[495]	7137.92	192.5
1037	S[382]	8493.52	282.5	1094	S[439]	7809.72	282.5	1151	S[496]	7125.92	282.5
1038	S[383]	8481.52	372.5	1095	S[440]	7797.72	372.5	1152	S[497]	7113.92	372.5
1039	S[384]	8469.53	192.5	1096	S[441]	7785.73	192.5	1153	S[498]	7101.93	192.5
1040	S[385]	8457.53	282.5	1097	S[442]	7773.73	282.5	1154	S[499]	7089.93	282.5
1041	S[386]	8445.54	372.5	1098	S[443]	7761.73	372.5	1155	S[500]	7077.93	372.5
1042	S[387]	8433.54	192.5	1099	S[444]	7749.74	192.5	1156	S[501]	7065.94	192.5
1043	S[388]	8421.54	282.5	1100	S[445]	7737.74	282.5	1157	S[502]	7053.94	282.5
1044	S[389]	8409.55	372.5	1101	S[446]	7725.75	372.5	1158	S[503]	7041.94	372.5
1045	S[390]	8397.55	192.5	1102	S[447]	7713.75	192.5	1159	S[504]	7029.95	192.5
1046	S[391]	8385.55	282.5	1103	S[448]	7701.75	282.5	1160	S[505]	7017.95	282.5
1047	S[392]	8373.56	372.5	1104	S[449]	7689.76	372.5	1161	S[506]	7005.96	372.5
1048	S[393]	8361.56	192.5	1105	S[450]	7677.76	192.5	1162	S[507]	6993.96	192.5
1049	S[394]	8349.56	282.5	1106	S[451]	7665.76	282.5	1163	S[508]	6981.96	282.5
1050	S[395]	8337.57	372.5	1107	S[452]	7653.77	372.5	1164	S[509]	6969.97	372.5
1051	S[396]	8325.57	192.5	1108	S[453]	7641.77	192.5	1165	S[510]	6957.97	192.5
1052	S[397]	8313.57	282.5	1109	S[454]	7629.77	282.5	1166	S[511]	6945.97	282.5
1053	S[398]	8301.58	372.5	1110	S[455]	7617.78	372.5	1167	S[512]	6933.98	372.5
1054	S[399]	8289.58	192.5	1111	S[456]	7605.78	192.5	1168	DUMMY[49]	6921.98	192.5
1055	S[400]	8277.58	282.5	1112	S[457]	7593.78	282.5	1169	DUMMY[50]	6909.98	282.5
1056	S[401]	8265.59	372.5	1113	S[458]	7581.79	372.5	1170	DUMMY[51]	6897.99	372.5
1057	S[402]	8253.59	192.5	1114	S[459]	7569.79	192.5	1171	DUMMY[52]	6885.99	192.5
1058	S[403]	8241.59	282.5	1115	S[460]	7557.79	282.5	1172	DUMMY[53]	6873.99	282.5
1059	S[404]	8229.60	372.5	1116	S[461]	7545.80	372.5	1173	DUMMY[54]	6862.00	372.5
1060	S[405]	8217.60	192.5	1117	S[462]	7533.80	192.5	1174	DUMMY[55]	6850.00	192.5
1061	S[406]	8205.61	282.5	1118	S[463]	7521.80	282.5	1175	DUMMY[56]	6838.00	282.5
1062	S[407]	8193.61	372.5	1119	S[464]	7509.81	372.5	1176	DUMMY[57]	6826.01	372.5
1063	S[408]	8181.61	192.5	1120	S[465]	7497.81	192.5	1177	DUMMY[58]	6814.01	192.5
1064	S[409]	8169.62	282.5	1121	S[466]	7485.82	282.5	1178	DUMMY[59]	6802.01	282.5
1065	S[410]	8157.62	372.5	1122	S[467]	7473.82	372.5	1179	DUMMY[60]	6790.02	372.5
1066	S[411]	8145.62	192.5	1123	S[468]	7461.82	192.5	1180	DUMMY[61]	6778.02	192.5
1067	S[412]	8133.63	282.5	1124	S[469]	7449.83	282.5	1181	DUMMY[62]	6766.03	282.5
1068	S[413]	8121.63	372.5	1125	S[470]	7437.83	372.5	1182	DUMMY[63]	6754.03	372.5
1069	S[414]	8109.63	192.5	1126	S[471]	7425.83	192.5	1183	DUMMY[64]	6742.03	192.5
1070	S[415]	8097.64	282.5	1127	S[472]	7413.84	282.5	1184	DUMMY[65]	6730.04	282.5
1071	S[416]	8085.64	372.5	1128	S[473]	7401.84	372.5	1185	DUMMY[66]	6718.04	372.5
1072	S[417]	8073.64	192.5	1129	S[474]	7389.84	192.5	1186	S[513]	6706.04	192.5
1073	S[418]	8061.65	282.5	1130	S[475]	7377.85	282.5	1187	S[514]	6694.05	282.5
1074	S[419]	8049.65	372.5	1131	S[476]	7365.85	372.5	1188	S[515]	6682.05	372.5
1075	S[420]	8037.65	192.5	1132	S[477]	7353.85	192.5	1189	S[516]	6670.05	192.5
1076	S[421]	8025.66	282.5	1133	S[478]	7341.86	282.5	1190	S[517]	6658.06	282.5
1077	S[422]	8013.66	372.5	1134	S[479]	7329.86	372.5	1191	S[518]	6646.06	372.5
1078	S[423]	8001.66	192.5	1135	S[480]	7317.86	192.5	1192	S[519]	6634.06	192.5
1079	S[424]	7989.67	282.5	1136	S[481]	7305.87	282.5	1193	S[520]	6622.07	282.5
1080	S[425]	7977.67	372.5	1137	S[482]	7293.87	372.5	1194	S[521]	6610.07	372.5
1081	S[426]	7965.68	192.5	1138	S[483]	7281.87	192.5	1195	S[522]	6598.07	192.5
1082	S[427]	7953.68	282.5	1139	S[484]	7269.88	282.5	1196	S[523]	6586.08	282.5
1083	S[428]	7941.68	372.5	1140	S[485]	7257.88	372.5	1197	S[524]	6574.08	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1198	S[525]	6562.08	192.5	1255	S[582]	5878.28	192.5	1312	S[639]	5194.48	192.5
1199	S[526]	6550.09	282.5	1256	S[583]	5866.29	282.5	1313	S[640]	5182.49	282.5
1200	S[527]	6538.09	372.5	1257	S[584]	5854.29	372.5	1314	S[641]	5170.49	372.5
1201	S[528]	6526.10	192.5	1258	S[585]	5842.29	192.5	1315	S[642]	5158.49	192.5
1202	S[529]	6514.10	282.5	1259	S[586]	5830.30	282.5	1316	S[643]	5146.50	282.5
1203	S[530]	6502.10	372.5	1260	S[587]	5818.30	372.5	1317	S[644]	5134.50	372.5
1204	S[531]	6490.11	192.5	1261	S[588]	5806.31	192.5	1318	S[645]	5122.51	192.5
1205	S[532]	6478.11	282.5	1262	S[589]	5794.31	282.5	1319	S[646]	5110.51	282.5
1206	S[533]	6466.11	372.5	1263	S[590]	5782.31	372.5	1320	S[647]	5098.51	372.5
1207	S[534]	6454.12	192.5	1264	S[591]	5770.32	192.5	1321	S[648]	5086.52	192.5
1208	S[535]	6442.12	282.5	1265	S[592]	5758.32	282.5	1322	S[649]	5074.52	282.5
1209	S[536]	6430.12	372.5	1266	S[593]	5746.32	372.5	1323	S[650]	5062.52	372.5
1210	S[537]	6418.13	192.5	1267	S[594]	5734.33	192.5	1324	S[651]	5050.53	192.5
1211	S[538]	6406.13	282.5	1268	S[595]	5722.33	282.5	1325	S[652]	5038.53	282.5
1212	S[539]	6394.13	372.5	1269	S[596]	5710.33	372.5	1326	S[653]	5026.53	372.5
1213	S[540]	6382.14	192.5	1270	S[597]	5698.34	192.5	1327	S[654]	5014.54	192.5
1214	S[541]	6370.14	282.5	1271	S[598]	5686.34	282.5	1328	S[655]	5002.54	282.5
1215	S[542]	6358.14	372.5	1272	S[599]	5674.34	372.5	1329	S[656]	4990.54	372.5
1216	S[543]	6346.15	192.5	1273	S[600]	5662.35	192.5	1330	S[657]	4978.55	192.5
1217	S[544]	6334.15	282.5	1274	S[601]	5650.35	282.5	1331	S[658]	4966.55	282.5
1218	S[545]	6322.15	372.5	1275	S[602]	5638.35	372.5	1332	S[659]	4954.55	372.5
1219	S[546]	6310.16	192.5	1276	S[603]	5626.36	192.5	1333	S[660]	4942.56	192.5
1220	S[547]	6298.16	282.5	1277	S[604]	5614.36	282.5	1334	S[661]	4930.56	282.5
1221	S[548]	6286.17	372.5	1278	S[605]	5602.36	372.5	1335	S[662]	4918.56	372.5
1222	S[549]	6274.17	192.5	1279	S[606]	5590.37	192.5	1336	S[663]	4906.57	192.5
1223	S[550]	6262.17	282.5	1280	S[607]	5578.37	282.5	1337	S[664]	4894.57	282.5
1224	S[551]	6250.18	372.5	1281	S[608]	5566.38	372.5	1338	S[665]	4882.58	372.5
1225	S[552]	6238.18	192.5	1282	S[609]	5554.38	192.5	1339	S[666]	4870.58	192.5
1226	S[553]	6226.18	282.5	1283	S[610]	5542.38	282.5	1340	S[667]	4858.58	282.5
1227	S[554]	6214.19	372.5	1284	S[611]	5530.39	372.5	1341	S[668]	4846.59	372.5
1228	S[555]	6202.19	192.5	1285	S[612]	5518.39	192.5	1342	S[669]	4834.59	192.5
1229	S[556]	6190.19	282.5	1286	S[613]	5506.39	282.5	1343	S[670]	4822.59	282.5
1230	S[557]	6178.20	372.5	1287	S[614]	5494.40	372.5	1344	S[671]	4810.60	372.5
1231	S[558]	6166.20	192.5	1288	S[615]	5482.40	192.5	1345	S[672]	4798.60	192.5
1232	S[559]	6154.20	282.5	1289	S[616]	5470.40	282.5	1346	S[673]	4786.60	282.5
1233	S[560]	6142.21	372.5	1290	S[617]	5458.41	372.5	1347	S[674]	4774.61	372.5
1234	S[561]	6130.21	192.5	1291	S[618]	5446.41	192.5	1348	S[675]	4762.61	192.5
1235	S[562]	6118.21	282.5	1292	S[619]	5434.41	282.5	1349	S[676]	4750.61	282.5
1236	S[563]	6106.22	372.5	1293	S[620]	5422.42	372.5	1350	S[677]	4738.62	372.5
1237	S[564]	6094.22	192.5	1294	S[621]	5410.42	192.5	1351	S[678]	4726.62	192.5
1238	S[565]	6082.22	282.5	1295	S[622]	5398.42	282.5	1352	S[679]	4714.62	282.5
1239	S[566]	6070.23	372.5	1296	S[623]	5386.43	372.5	1353	S[680]	4702.63	372.5
1240	S[567]	6058.23	192.5	1297	S[624]	5374.43	192.5	1354	S[681]	4690.63	192.5
1241	S[568]	6046.24	282.5	1298	S[625]	5362.44	282.5	1355	S[682]	4678.63	282.5
1242	S[569]	6034.24	372.5	1299	S[626]	5350.44	372.5	1356	S[683]	4666.64	372.5
1243	S[570]	6022.24	192.5	1300	S[627]	5338.44	192.5	1357	S[684]	4654.64	192.5
1244	S[571]	6010.25	282.5	1301	S[628]	5326.45	282.5	1358	S[685]	4642.65	282.5
1245	S[572]	5998.25	372.5	1302	S[629]	5314.45	372.5	1359	S[686]	4630.65	372.5
1246	S[573]	5986.25	192.5	1303	S[630]	5302.45	192.5	1360	S[687]	4618.65	192.5
1247	S[574]	5974.26	282.5	1304	S[631]	5290.46	282.5	1361	S[688]	4606.66	282.5
1248	S[575]	5962.26	372.5	1305	S[632]	5278.46	372.5	1362	S[689]	4594.66	372.5
1249	S[576]	5950.26	192.5	1306	S[633]	5266.46	192.5	1363	S[690]	4582.66	192.5
1250	S[577]	5938.27	282.5	1307	S[634]	5254.47	282.5	1364	S[691]	4570.67	282.5
1251	S[578]	5926.27	372.5	1308	S[635]	5242.47	372.5	1365	S[692]	4558.67	372.5
1252	S[579]	5914.27	192.5	1309	S[636]	5230.47	192.5	1366	S[693]	4546.67	192.5
1253	S[580]	5902.28	282.5	1310	S[637]	5218.48	282.5	1367	S[694]	4534.68	282.5
1254	S[581]	5890.28	372.5	1311	S[638]	5206.48	372.5	1368	S[695]	4522.68	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1369	S[696]	4510.68	192.5	1426	S[753]	3826.88	192.5	1483	S[810]	3143.08	192.5
1370	S[697]	4498.69	282.5	1427	S[754]	3814.89	282.5	1484	S[811]	3131.09	282.5
1371	S[698]	4486.69	372.5	1428	S[755]	3802.89	372.5	1485	S[812]	3119.09	372.5
1372	S[699]	4474.69	192.5	1429	S[756]	3790.89	192.5	1486	S[813]	3107.09	192.5
1373	S[700]	4462.70	282.5	1430	S[757]	3778.90	282.5	1487	S[814]	3095.10	282.5
1374	S[701]	4450.70	372.5	1431	S[758]	3766.90	372.5	1488	S[815]	3083.10	372.5
1375	S[702]	4438.70	192.5	1432	S[759]	3754.90	192.5	1489	S[816]	3071.10	192.5
1376	S[703]	4426.71	282.5	1433	S[760]	3742.91	282.5	1490	S[817]	3059.11	282.5
1377	S[704]	4414.71	372.5	1434	S[761]	3730.91	372.5	1491	S[818]	3047.11	372.5
1378	S[705]	4402.72	192.5	1435	S[762]	3718.91	192.5	1492	S[819]	3035.11	192.5
1379	S[706]	4390.72	282.5	1436	S[763]	3706.92	282.5	1493	S[820]	3023.12	282.5
1380	S[707]	4378.72	372.5	1437	S[764]	3694.92	372.5	1494	S[821]	3011.12	372.5
1381	S[708]	4366.73	192.5	1438	S[765]	3682.93	192.5	1495	S[822]	2999.12	192.5
1382	S[709]	4354.73	282.5	1439	S[766]	3670.93	282.5	1496	S[823]	2987.13	282.5
1383	S[710]	4342.73	372.5	1440	S[767]	3658.93	372.5	1497	S[824]	2975.13	372.5
1384	S[711]	4330.74	192.5	1441	S[768]	3646.94	192.5	1498	S[825]	2963.14	192.5
1385	S[712]	4318.74	282.5	1442	S[769]	3634.94	282.5	1499	S[826]	2951.14	282.5
1386	S[713]	4306.74	372.5	1443	S[770]	3622.94	372.5	1500	S[827]	2939.14	372.5
1387	S[714]	4294.75	192.5	1444	S[771]	3610.95	192.5	1501	S[828]	2927.15	192.5
1388	S[715]	4282.75	282.5	1445	S[772]	3598.95	282.5	1502	S[829]	2915.15	282.5
1389	S[716]	4270.75	372.5	1446	S[773]	3586.95	372.5	1503	S[830]	2903.15	372.5
1390	S[717]	4258.76	192.5	1447	S[774]	3574.96	192.5	1504	S[831]	2891.16	192.5
1391	S[718]	4246.76	282.5	1448	S[775]	3562.96	282.5	1505	S[832]	2879.16	282.5
1392	S[719]	4234.76	372.5	1449	S[776]	3550.96	372.5	1506	S[833]	2867.16	372.5
1393	S[720]	4222.77	192.5	1450	S[777]	3538.97	192.5	1507	S[834]	2855.17	192.5
1394	S[721]	4210.77	282.5	1451	S[778]	3526.97	282.5	1508	S[835]	2843.17	282.5
1395	S[722]	4198.77	372.5	1452	S[779]	3514.97	372.5	1509	S[836]	2831.17	372.5
1396	S[723]	4186.78	192.5	1453	S[780]	3502.98	192.5	1510	S[837]	2819.18	192.5
1397	S[724]	4174.78	282.5	1454	S[781]	3490.98	282.5	1511	S[838]	2807.18	282.5
1398	S[725]	4162.79	372.5	1455	S[782]	3478.98	372.5	1512	S[839]	2795.18	372.5
1399	S[726]	4150.79	192.5	1456	S[783]	3466.99	192.5	1513	S[840]	2783.19	192.5
1400	S[727]	4138.79	282.5	1457	S[784]	3454.99	282.5	1514	S[841]	2771.19	282.5
1401	S[728]	4126.80	372.5	1458	S[785]	3443.00	372.5	1515	S[842]	2759.19	372.5
1402	S[729]	4114.80	192.5	1459	S[786]	3431.00	192.5	1516	S[843]	2747.20	192.5
1403	S[730]	4102.80	282.5	1460	S[787]	3419.00	282.5	1517	S[844]	2735.20	282.5
1404	S[731]	4090.81	372.5	1461	S[788]	3407.01	372.5	1518	S[845]	2723.21	372.5
1405	S[732]	4078.81	192.5	1462	S[789]	3395.01	192.5	1519	S[846]	2711.21	192.5
1406	S[733]	4066.81	282.5	1463	S[790]	3383.01	282.5	1520	S[847]	2699.21	282.5
1407	S[734]	4054.82	372.5	1464	S[791]	3371.02	372.5	1521	S[848]	2687.22	372.5
1408	S[735]	4042.82	192.5	1465	S[792]	3359.02	192.5	1522	S[849]	2675.22	192.5
1409	S[736]	4030.82	282.5	1466	S[793]	3347.02	282.5	1523	S[850]	2663.22	282.5
1410	S[737]	4018.83	372.5	1467	S[794]	3335.03	372.5	1524	S[851]	2651.23	372.5
1411	S[738]	4006.83	192.5	1468	S[795]	3323.03	192.5	1525	S[852]	2639.23	192.5
1412	S[739]	3994.83	282.5	1469	S[796]	3311.03	282.5	1526	S[853]	2627.23	282.5
1413	S[740]	3982.84	372.5	1470	S[797]	3299.04	372.5	1527	S[854]	2615.24	372.5
1414	S[741]	3970.84	192.5	1471	S[798]	3287.04	192.5	1528	S[855]	2603.24	192.5
1415	S[742]	3958.84	282.5	1472	S[799]	3275.04	282.5	1529	S[856]	2591.24	282.5
1416	S[743]	3946.85	372.5	1473	S[800]	3263.05	372.5	1530	S[857]	2579.25	372.5
1417	S[744]	3934.85	192.5	1474	S[801]	3251.05	192.5	1531	S[858]	2567.25	192.5
1418	S[745]	3922.86	282.5	1475	S[802]	3239.05	282.5	1532	S[859]	2555.25	282.5
1419	S[746]	3910.86	372.5	1476	S[803]	3227.06	372.5	1533	S[860]	2543.26	372.5
1420	S[747]	3898.86	192.5	1477	S[804]	3215.06	192.5	1534	S[861]	2531.26	192.5
1421	S[748]	3886.87	282.5	1478	S[805]	3203.07	282.5	1535	S[862]	2519.26	282.5
1422	S[749]	3874.87	372.5	1479	S[806]	3191.07	372.5	1536	S[863]	2507.27	372.5
1423	S[750]	3862.87	192.5	1480	S[807]	3179.07	192.5	1537	S[864]	2495.27	192.5
1424	S[751]	3850.88	282.5	1481	S[808]	3167.08	282.5	1538	S[865]	2483.28	282.5
1425	S[752]	3838.88	372.5	1482	S[809]	3155.08	372.5	1539	S[866]	2471.28	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1540	S[867]	2459.28	192.5	1597	S[924]	1775.48	192.5	1654	S[981]	1091.68	192.5
1541	S[868]	2447.29	282.5	1598	S[925]	1763.49	282.5	1655	S[982]	1079.68	282.5
1542	S[869]	2435.29	372.5	1599	S[926]	1751.49	372.5	1656	S[983]	1067.69	372.5
1543	S[870]	2423.29	192.5	1600	S[927]	1739.49	192.5	1657	S[984]	1055.69	192.5
1544	S[871]	2411.30	282.5	1601	S[928]	1727.50	282.5	1658	S[985]	1043.70	282.5
1545	S[872]	2399.30	372.5	1602	S[929]	1715.50	372.5	1659	S[986]	1031.70	372.5
1546	S[873]	2387.30	192.5	1603	S[930]	1703.50	192.5	1660	S[987]	1019.70	192.5
1547	S[874]	2375.31	282.5	1604	S[931]	1691.51	282.5	1661	S[988]	1007.71	282.5
1548	S[875]	2363.31	372.5	1605	S[932]	1679.51	372.5	1662	S[989]	995.71	372.5
1549	S[876]	2351.31	192.5	1606	S[933]	1667.51	192.5	1663	S[990]	983.71	192.5
1550	S[877]	2339.32	282.5	1607	S[934]	1655.52	282.5	1664	S[991]	971.72	282.5
1551	S[878]	2327.32	372.5	1608	S[935]	1643.52	372.5	1665	S[992]	959.72	372.5
1552	S[879]	2315.32	192.5	1609	S[936]	1631.52	192.5	1666	S[993]	947.72	192.5
1553	S[880]	2303.33	282.5	1610	S[937]	1619.53	282.5	1667	S[994]	935.73	282.5
1554	S[881]	2291.33	372.5	1611	S[938]	1607.53	372.5	1668	S[995]	923.73	372.5
1555	S[882]	2279.33	192.5	1612	S[939]	1595.53	192.5	1669	S[996]	911.73	192.5
1556	S[883]	2267.34	282.5	1613	S[940]	1583.54	282.5	1670	S[997]	899.74	282.5
1557	S[884]	2255.34	372.5	1614	S[941]	1571.54	372.5	1671	S[998]	887.74	372.5
1558	S[885]	2243.35	192.5	1615	S[942]	1559.54	192.5	1672	S[999]	875.74	192.5
1559	S[886]	2231.35	282.5	1616	S[943]	1547.55	282.5	1673	S[1000]	863.75	282.5
1560	S[887]	2219.35	372.5	1617	S[944]	1535.55	372.5	1674	S[1001]	851.75	372.5
1561	S[888]	2207.36	192.5	1618	S[945]	1523.56	192.5	1675	S[1002]	839.75	192.5
1562	S[889]	2195.36	282.5	1619	S[946]	1511.56	282.5	1676	S[1003]	827.76	282.5
1563	S[890]	2183.36	372.5	1620	S[947]	1499.56	372.5	1677	S[1004]	815.76	372.5
1564	S[891]	2171.37	192.5	1621	S[948]	1487.57	192.5	1678	S[1005]	803.77	192.5
1565	S[892]	2159.37	282.5	1622	S[949]	1475.57	282.5	1679	S[1006]	791.77	282.5
1566	S[893]	2147.37	372.5	1623	S[950]	1463.57	372.5	1680	S[1007]	779.77	372.5
1567	S[894]	2135.38	192.5	1624	S[951]	1451.58	192.5	1681	S[1008]	767.78	192.5
1568	S[895]	2123.38	282.5	1625	S[952]	1439.58	282.5	1682	S[1009]	755.78	282.5
1569	S[896]	2111.38	372.5	1626	S[953]	1427.58	372.5	1683	S[1010]	743.78	372.5
1570	S[897]	2099.39	192.5	1627	S[954]	1415.59	192.5	1684	S[1011]	731.79	192.5
1571	S[898]	2087.39	282.5	1628	S[955]	1403.59	282.5	1685	S[1012]	719.79	282.5
1572	S[899]	2075.39	372.5	1629	S[956]	1391.59	372.5	1686	S[1013]	707.79	372.5
1573	S[900]	2063.40	192.5	1630	S[957]	1379.60	192.5	1687	S[1014]	695.80	192.5
1574	S[901]	2051.40	282.5	1631	S[958]	1367.60	282.5	1688	S[1015]	683.80	282.5
1575	S[902]	2039.40	372.5	1632	S[959]	1355.60	372.5	1689	S[1016]	671.80	372.5
1576	S[903]	2027.41	192.5	1633	S[960]	1343.61	192.5	1690	S[1017]	659.81	192.5
1577	S[904]	2015.41	282.5	1634	S[961]	1331.61	282.5	1691	S[1018]	647.81	282.5
1578	S[905]	2003.42	372.5	1635	S[962]	1319.61	372.5	1692	S[1019]	635.81	372.5
1579	S[906]	1991.42	192.5	1636	S[963]	1307.62	192.5	1693	S[1020]	623.82	192.5
1580	S[907]	1979.42	282.5	1637	S[964]	1295.62	282.5	1694	S[1021]	611.82	282.5
1581	S[908]	1967.43	372.5	1638	S[965]	1283.63	372.5	1695	S[1022]	599.82	372.5
1582	S[909]	1955.43	192.5	1639	S[966]	1271.63	192.5	1696	S[1023]	587.83	192.5
1583	S[910]	1943.43	282.5	1640	S[967]	1259.63	282.5	1697	S[1024]	575.83	282.5
1584	S[911]	1931.44	372.5	1641	S[968]	1247.64	372.5	1698	S[1025]	563.84	372.5
1585	S[912]	1919.44	192.5	1642	S[969]	1235.64	192.5	1699	DUMMY[67]	527.85	372.5
1586	S[913]	1907.44	282.5	1643	S[970]	1223.64	282.5	1700	DUMMY[68]	491.86	372.5
1587	S[914]	1895.45	372.5	1644	S[971]	1211.65	372.5	1701	DUMMY[69]	455.87	372.5
1588	S[915]	1883.45	192.5	1645	S[972]	1199.65	192.5	1702	DUMMY[70]	419.88	372.5
1589	S[916]	1871.45	282.5	1646	S[973]	1187.65	282.5	1703	DUMMY[71]	383.89	372.5
1590	S[917]	1859.46	372.5	1647	S[974]	1175.66	372.5	1704	DUMMY[72]	347.90	372.5
1591	S[918]	1847.46	192.5	1648	S[975]	1163.66	192.5	1705	DUMMY[73]	311.91	372.5
1592	S[919]	1835.46	282.5	1649	S[976]	1151.66	282.5	1706	DUMMY[74]	275.92	372.5
1593	S[920]	1823.47	372.5	1650	S[977]	1139.67	372.5	1707	DUMMY[75]	239.93	372.5
1594	S[921]	1811.47	192.5	1651	S[978]	1127.67	192.5	1708	DUMMY[76]	203.94	372.5
1595	S[922]	1799.47	282.5	1652	S[979]	1115.67	282.5	1709	DUMMY[77]	167.95	372.5
1596	S[923]	1787.48	372.5	1653	S[980]	1103.68	372.5	1710	DUMMY[78]	131.96	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1711	DUMMY[79]	95.97	372.5	1768	S[1065]	-995.71	192.5	1825	S[1122]	-1679.51	192.5
1712	DUMMY[80]	59.98	372.5	1769	S[1066]	-1007.71	282.5	1826	S[1123]	-1691.51	282.5
1713	DUMMY[81]	23.99	372.5	1770	S[1067]	-1019.70	372.5	1827	S[1124]	-1703.50	372.5
1714	DUMMY[82]	-12.00	372.5	1771	S[1068]	-1031.70	192.5	1828	S[1125]	-1715.50	192.5
1715	DUMMY[83]	-47.99	372.5	1772	S[1069]	-1043.70	282.5	1829	S[1126]	-1727.50	282.5
1716	DUMMY[84]	-83.98	372.5	1773	S[1070]	-1055.69	372.5	1830	S[1127]	-1739.49	372.5
1717	DUMMY[85]	-119.96	372.5	1774	S[1071]	-1067.69	192.5	1831	S[1128]	-1751.49	192.5
1718	DUMMY[86]	-155.95	372.5	1775	S[1072]	-1079.68	282.5	1832	S[1129]	-1763.49	282.5
1719	DUMMY[87]	-191.94	372.5	1776	S[1073]	-1091.68	372.5	1833	S[1130]	-1775.48	372.5
1720	DUMMY[88]	-227.93	372.5	1777	S[1074]	-1103.68	192.5	1834	S[1131]	-1787.48	192.5
1721	DUMMY[89]	-263.92	372.5	1778	S[1075]	-1115.67	282.5	1835	S[1132]	-1799.47	282.5
1722	DUMMY[90]	-299.91	372.5	1779	S[1076]	-1127.67	372.5	1836	S[1133]	-1811.47	372.5
1723	DUMMY[91]	-335.90	372.5	1780	S[1077]	-1139.67	192.5	1837	S[1134]	-1823.47	192.5
1724	DUMMY[92]	-371.89	372.5	1781	S[1078]	-1151.66	282.5	1838	S[1135]	-1835.46	282.5
1725	DUMMY[93]	-407.88	372.5	1782	S[1079]	-1163.66	372.5	1839	S[1136]	-1847.46	372.5
1726	DUMMY[94]	-443.87	372.5	1783	S[1080]	-1175.66	192.5	1840	S[1137]	-1859.46	192.5
1727	DUMMY[95]	-479.86	372.5	1784	S[1081]	-1187.65	282.5	1841	S[1138]	-1871.45	282.5
1728	DUMMY[96]	-515.85	372.5	1785	S[1082]	-1199.65	372.5	1842	S[1139]	-1883.45	372.5
1729	S[1026]	-527.85	192.5	1786	S[1083]	-1211.65	192.5	1843	S[1140]	-1895.45	192.5
1730	S[1027]	-539.84	282.5	1787	S[1084]	-1223.64	282.5	1844	S[1141]	-1907.44	282.5
1731	S[1028]	-551.84	372.5	1788	S[1085]	-1235.64	372.5	1845	S[1142]	-1919.44	372.5
1732	S[1029]	-563.84	192.5	1789	S[1086]	-1247.64	192.5	1846	S[1143]	-1931.44	192.5
1733	S[1030]	-575.83	282.5	1790	S[1087]	-1259.63	282.5	1847	S[1144]	-1943.43	282.5
1734	S[1031]	-587.83	372.5	1791	S[1088]	-1271.63	372.5	1848	S[1145]	-1955.43	372.5
1735	S[1032]	-599.82	192.5	1792	S[1089]	-1283.63	192.5	1849	S[1146]	-1967.43	192.5
1736	S[1033]	-611.82	282.5	1793	S[1090]	-1295.62	282.5	1850	S[1147]	-1979.42	282.5
1737	S[1034]	-623.82	372.5	1794	S[1091]	-1307.62	372.5	1851	S[1148]	-1991.42	372.5
1738	S[1035]	-635.81	192.5	1795	S[1092]	-1319.61	192.5	1852	S[1149]	-2003.42	192.5
1739	S[1036]	-647.81	282.5	1796	S[1093]	-1331.61	282.5	1853	S[1150]	-2015.41	282.5
1740	S[1037]	-659.81	372.5	1797	S[1094]	-1343.61	372.5	1854	S[1151]	-2027.41	372.5
1741	S[1038]	-671.80	192.5	1798	S[1095]	-1355.60	192.5	1855	S[1152]	-2039.40	192.5
1742	S[1039]	-683.80	282.5	1799	S[1096]	-1367.60	282.5	1856	S[1153]	-2051.40	282.5
1743	S[1040]	-695.80	372.5	1800	S[1097]	-1379.60	372.5	1857	S[1154]	-2063.40	372.5
1744	S[1041]	-707.79	192.5	1801	S[1098]	-1391.59	192.5	1858	S[1155]	-2075.39	192.5
1745	S[1042]	-719.79	282.5	1802	S[1099]	-1403.59	282.5	1859	S[1156]	-2087.39	282.5
1746	S[1043]	-731.79	372.5	1803	S[1100]	-1415.59	372.5	1860	S[1157]	-2099.39	372.5
1747	S[1044]	-743.78	192.5	1804	S[1101]	-1427.58	192.5	1861	S[1158]	-2111.38	192.5
1748	S[1045]	-755.78	282.5	1805	S[1102]	-1439.58	282.5	1862	S[1159]	-2123.38	282.5
1749	S[1046]	-767.78	372.5	1806	S[1103]	-1451.58	372.5	1863	S[1160]	-2135.38	372.5
1750	S[1047]	-779.77	192.5	1807	S[1104]	-1463.57	192.5	1864	S[1161]	-2147.37	192.5
1751	S[1048]	-791.77	282.5	1808	S[1105]	-1475.57	282.5	1865	S[1162]	-2159.37	282.5
1752	S[1049]	-803.77	372.5	1809	S[1106]	-1487.57	372.5	1866	S[1163]	-2171.37	372.5
1753	S[1050]	-815.76	192.5	1810	S[1107]	-1499.56	192.5	1867	S[1164]	-2183.36	192.5
1754	S[1051]	-827.76	282.5	1811	S[1108]	-1511.56	282.5	1868	S[1165]	-2195.36	282.5
1755	S[1052]	-839.75	372.5	1812	S[1109]	-1523.56	372.5	1869	S[1166]	-2207.36	372.5
1756	S[1053]	-851.75	192.5	1813	S[1110]	-1535.55	192.5	1870	S[1167]	-2219.35	192.5
1757	S[1054]	-863.75	282.5	1814	S[1111]	-1547.55	282.5	1871	S[1168]	-2231.35	282.5
1758	S[1055]	-875.74	372.5	1815	S[1112]	-1559.54	372.5	1872	S[1169]	-2243.35	372.5
1759	S[1056]	-887.74	192.5	1816	S[1113]	-1571.54	192.5	1873	S[1170]	-2255.34	192.5
1760	S[1057]	-899.74	282.5	1817	S[1114]	-1583.54	282.5	1874	S[1171]	-2267.34	282.5
1761	S[1058]	-911.73	372.5	1818	S[1115]	-1595.53	372.5	1875	S[1172]	-2279.33	372.5
1762	S[1059]	-923.73	192.5	1819	S[1116]	-1607.53	192.5	1876	S[1173]	-2291.33	192.5
1763	S[1060]	-935.73	282.5	1820	S[1117]	-1619.53	282.5	1877	S[1174]	-2303.33	282.5
1764	S[1061]	-947.72	372.5	1821	S[1118]	-1631.52	372.5	1878	S[1175]	-2315.32	372.5
1765	S[1062]	-959.72	192.5	1822	S[1119]	-1643.52	192.5	1879	S[1176]	-2327.32	192.5
1766	S[1063]	-971.72	282.5	1823	S[1120]	-1655.52	282.5	1880	S[1177]	-2339.32	282.5
1767	S[1064]	-983.71	372.5	1824	S[1121]	-1667.51	372.5	1881	S[1178]	-2351.31	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1882	S[1179]	-2363.31	192.5	1939	S[1236]	-3047.11	192.5	1996	S[1293]	-3730.91	192.5
1883	S[1180]	-2375.31	282.5	1940	S[1237]	-3059.11	282.5	1997	S[1294]	-3742.91	282.5
1884	S[1181]	-2387.30	372.5	1941	S[1238]	-3071.10	372.5	1998	S[1295]	-3754.90	372.5
1885	S[1182]	-2399.30	192.5	1942	S[1239]	-3083.10	192.5	1999	S[1296]	-3766.90	192.5
1886	S[1183]	-2411.30	282.5	1943	S[1240]	-3095.10	282.5	2000	S[1297]	-3778.90	282.5
1887	S[1184]	-2423.29	372.5	1944	S[1241]	-3107.09	372.5	2001	S[1298]	-3790.89	372.5
1888	S[1185]	-2435.29	192.5	1945	S[1242]	-3119.09	192.5	2002	S[1299]	-3802.89	192.5
1889	S[1186]	-2447.29	282.5	1946	S[1243]	-3131.09	282.5	2003	S[1300]	-3814.89	282.5
1890	S[1187]	-2459.28	372.5	1947	S[1244]	-3143.08	372.5	2004	S[1301]	-3826.88	372.5
1891	S[1188]	-2471.28	192.5	1948	S[1245]	-3155.08	192.5	2005	S[1302]	-3838.88	192.5
1892	S[1189]	-2483.28	282.5	1949	S[1246]	-3167.08	282.5	2006	S[1303]	-3850.88	282.5
1893	S[1190]	-2495.27	372.5	1950	S[1247]	-3179.07	372.5	2007	S[1304]	-3862.87	372.5
1894	S[1191]	-2507.27	192.5	1951	S[1248]	-3191.07	192.5	2008	S[1305]	-3874.87	192.5
1895	S[1192]	-2519.26	282.5	1952	S[1249]	-3203.07	282.5	2009	S[1306]	-3886.87	282.5
1896	S[1193]	-2531.26	372.5	1953	S[1250]	-3215.06	372.5	2010	S[1307]	-3898.86	372.5
1897	S[1194]	-2543.26	192.5	1954	S[1251]	-3227.06	192.5	2011	S[1308]	-3910.86	192.5
1898	S[1195]	-2555.25	282.5	1955	S[1252]	-3239.05	282.5	2012	S[1309]	-3922.86	282.5
1899	S[1196]	-2567.25	372.5	1956	S[1253]	-3251.05	372.5	2013	S[1310]	-3934.85	372.5
1900	S[1197]	-2579.25	192.5	1957	S[1254]	-3263.05	192.5	2014	S[1311]	-3946.85	192.5
1901	S[1198]	-2591.24	282.5	1958	S[1255]	-3275.04	282.5	2015	S[1312]	-3958.84	282.5
1902	S[1199]	-2603.24	372.5	1959	S[1256]	-3287.04	372.5	2016	S[1313]	-3970.84	372.5
1903	S[1200]	-2615.24	192.5	1960	S[1257]	-3299.04	192.5	2017	S[1314]	-3982.84	192.5
1904	S[1201]	-2627.23	282.5	1961	S[1258]	-3311.03	282.5	2018	S[1315]	-3994.83	282.5
1905	S[1202]	-2639.23	372.5	1962	S[1259]	-3323.03	372.5	2019	S[1316]	-4006.83	372.5
1906	S[1203]	-2651.23	192.5	1963	S[1260]	-3335.03	192.5	2020	S[1317]	-4018.83	192.5
1907	S[1204]	-2663.22	282.5	1964	S[1261]	-3347.02	282.5	2021	S[1318]	-4030.82	282.5
1908	S[1205]	-2675.22	372.5	1965	S[1262]	-3359.02	372.5	2022	S[1319]	-4042.82	372.5
1909	S[1206]	-2687.22	192.5	1966	S[1263]	-3371.02	192.5	2023	S[1320]	-4054.82	192.5
1910	S[1207]	-2699.21	282.5	1967	S[1264]	-3383.01	282.5	2024	S[1321]	-4066.81	282.5
1911	S[1208]	-2711.21	372.5	1968	S[1265]	-3395.01	372.5	2025	S[1322]	-4078.81	372.5
1912	S[1209]	-2723.21	192.5	1969	S[1266]	-3407.01	192.5	2026	S[1323]	-4090.81	192.5
1913	S[1210]	-2735.20	282.5	1970	S[1267]	-3419.00	282.5	2027	S[1324]	-4102.80	282.5
1914	S[1211]	-2747.20	372.5	1971	S[1268]	-3431.00	372.5	2028	S[1325]	-4114.80	372.5
1915	S[1212]	-2759.19	192.5	1972	S[1269]	-3443.00	192.5	2029	S[1326]	-4126.80	192.5
1916	S[1213]	-2771.19	282.5	1973	S[1270]	-3454.99	282.5	2030	S[1327]	-4138.79	282.5
1917	S[1214]	-2783.19	372.5	1974	S[1271]	-3466.99	372.5	2031	S[1328]	-4150.79	372.5
1918	S[1215]	-2795.18	192.5	1975	S[1272]	-3478.98	192.5	2032	S[1329]	-4162.79	192.5
1919	S[1216]	-2807.18	282.5	1976	S[1273]	-3490.98	282.5	2033	S[1330]	-4174.78	282.5
1920	S[1217]	-2819.18	372.5	1977	S[1274]	-3502.98	372.5	2034	S[1331]	-4186.78	372.5
1921	S[1218]	-2831.17	192.5	1978	S[1275]	-3514.97	192.5	2035	S[1332]	-4198.77	192.5
1922	S[1219]	-2843.17	282.5	1979	S[1276]	-3526.97	282.5	2036	S[1333]	-4210.77	282.5
1923	S[1220]	-2855.17	372.5	1980	S[1277]	-3538.97	372.5	2037	S[1334]	-4222.77	372.5
1924	S[1221]	-2867.16	192.5	1981	S[1278]	-3550.96	192.5	2038	S[1335]	-4234.76	192.5
1925	S[1222]	-2879.16	282.5	1982	S[1279]	-3562.96	282.5	2039	S[1336]	-4246.76	282.5
1926	S[1223]	-2891.16	372.5	1983	S[1280]	-3574.96	372.5	2040	S[1337]	-4258.76	372.5
1927	S[1224]	-2903.15	192.5	1984	S[1281]	-3586.95	192.5	2041	S[1338]	-4270.75	192.5
1928	S[1225]	-2915.15	282.5	1985	S[1282]	-3598.95	282.5	2042	S[1339]	-4282.75	282.5
1929	S[1226]	-2927.15	372.5	1986	S[1283]	-3610.95	372.5	2043	S[1340]	-4294.75	372.5
1930	S[1227]	-2939.14	192.5	1987	S[1284]	-3622.94	192.5	2044	S[1341]	-4306.74	192.5
1931	S[1228]	-2951.14	282.5	1988	S[1285]	-3634.94	282.5	2045	S[1342]	-4318.74	282.5
1932	S[1229]	-2963.14	372.5	1989	S[1286]	-3646.94	372.5	2046	S[1343]	-4330.74	372.5
1933	S[1230]	-2975.13	192.5	1990	S[1287]	-3658.93	192.5	2047	S[1344]	-4342.73	192.5
1934	S[1231]	-2987.13	282.5	1991	S[1288]	-3670.93	282.5	2048	S[1345]	-4354.73	282.5
1935	S[1232]	-2999.12	372.5	1992	S[1289]	-3682.93	372.5	2049	S[1346]	-4366.73	372.5
1936	S[1233]	-3011.12	192.5	1993	S[1290]	-3694.92	192.5	2050	S[1347]	-4378.72	192.5
1937	S[1234]	-3023.12	282.5	1994	S[1291]	-3706.92	282.5	2051	S[1348]	-4390.72	282.5
1938	S[1235]	-3035.11	372.5	1995	S[1292]	-3718.91	372.5	2052	S[1349]	-4402.72	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2053	S[1350]	-4414.71	192.5	2110	S[1407]	-5098.51	192.5	2167	S[1464]	-5782.31	192.5
2054	S[1351]	-4426.71	282.5	2111	S[1408]	-5110.51	282.5	2168	S[1465]	-5794.31	282.5
2055	S[1352]	-4438.70	372.5	2112	S[1409]	-5122.51	372.5	2169	S[1466]	-5806.31	372.5
2056	S[1353]	-4450.70	192.5	2113	S[1410]	-5134.50	192.5	2170	S[1467]	-5818.30	192.5
2057	S[1354]	-4462.70	282.5	2114	S[1411]	-5146.50	282.5	2171	S[1468]	-5830.30	282.5
2058	S[1355]	-4474.69	372.5	2115	S[1412]	-5158.49	372.5	2172	S[1469]	-5842.29	372.5
2059	S[1356]	-4486.69	192.5	2116	S[1413]	-5170.49	192.5	2173	S[1470]	-5854.29	192.5
2060	S[1357]	-4498.69	282.5	2117	S[1414]	-5182.49	282.5	2174	S[1471]	-5866.29	282.5
2061	S[1358]	-4510.68	372.5	2118	S[1415]	-5194.48	372.5	2175	S[1472]	-5878.28	372.5
2062	S[1359]	-4522.68	192.5	2119	S[1416]	-5206.48	192.5	2176	S[1473]	-5890.28	192.5
2063	S[1360]	-4534.68	282.5	2120	S[1417]	-5218.48	282.5	2177	S[1474]	-5902.28	282.5
2064	S[1361]	-4546.67	372.5	2121	S[1418]	-5230.47	372.5	2178	S[1475]	-5914.27	372.5
2065	S[1362]	-4558.67	192.5	2122	S[1419]	-5242.47	192.5	2179	S[1476]	-5926.27	192.5
2066	S[1363]	-4570.67	282.5	2123	S[1420]	-5254.47	282.5	2180	S[1477]	-5938.27	282.5
2067	S[1364]	-4582.66	372.5	2124	S[1421]	-5266.46	372.5	2181	S[1478]	-5950.26	372.5
2068	S[1365]	-4594.66	192.5	2125	S[1422]	-5278.46	192.5	2182	S[1479]	-5962.26	192.5
2069	S[1366]	-4606.66	282.5	2126	S[1423]	-5290.46	282.5	2183	S[1480]	-5974.26	282.5
2070	S[1367]	-4618.65	372.5	2127	S[1424]	-5302.45	372.5	2184	S[1481]	-5986.25	372.5
2071	S[1368]	-4630.65	192.5	2128	S[1425]	-5314.45	192.5	2185	S[1482]	-5998.25	192.5
2072	S[1369]	-4642.65	282.5	2129	S[1426]	-5326.45	282.5	2186	S[1483]	-6010.25	282.5
2073	S[1370]	-4654.64	372.5	2130	S[1427]	-5338.44	372.5	2187	S[1484]	-6022.24	372.5
2074	S[1371]	-4666.64	192.5	2131	S[1428]	-5350.44	192.5	2188	S[1485]	-6034.24	192.5
2075	S[1372]	-4678.63	282.5	2132	S[1429]	-5362.44	282.5	2189	S[1486]	-6046.24	282.5
2076	S[1373]	-4690.63	372.5	2133	S[1430]	-5374.43	372.5	2190	S[1487]	-6058.23	372.5
2077	S[1374]	-4702.63	192.5	2134	S[1431]	-5386.43	192.5	2191	S[1488]	-6070.23	192.5
2078	S[1375]	-4714.62	282.5	2135	S[1432]	-5398.42	282.5	2192	S[1489]	-6082.22	282.5
2079	S[1376]	-4726.62	372.5	2136	S[1433]	-5410.42	372.5	2193	S[1490]	-6094.22	372.5
2080	S[1377]	-4738.62	192.5	2137	S[1434]	-5422.42	192.5	2194	S[1491]	-6106.22	192.5
2081	S[1378]	-4750.61	282.5	2138	S[1435]	-5434.41	282.5	2195	S[1492]	-6118.21	282.5
2082	S[1379]	-4762.61	372.5	2139	S[1436]	-5446.41	372.5	2196	S[1493]	-6130.21	372.5
2083	S[1380]	-4774.61	192.5	2140	S[1437]	-5458.41	192.5	2197	S[1494]	-6142.21	192.5
2084	S[1381]	-4786.60	282.5	2141	S[1438]	-5470.40	282.5	2198	S[1495]	-6154.20	282.5
2085	S[1382]	-4798.60	372.5	2142	S[1439]	-5482.40	372.5	2199	S[1496]	-6166.20	372.5
2086	S[1383]	-4810.60	192.5	2143	S[1440]	-5494.40	192.5	2200	S[1497]	-6178.20	192.5
2087	S[1384]	-4822.59	282.5	2144	S[1441]	-5506.39	282.5	2201	S[1498]	-6190.19	282.5
2088	S[1385]	-4834.59	372.5	2145	S[1442]	-5518.39	372.5	2202	S[1499]	-6202.19	372.5
2089	S[1386]	-4846.59	192.5	2146	S[1443]	-5530.39	192.5	2203	S[1500]	-6214.19	192.5
2090	S[1387]	-4858.58	282.5	2147	S[1444]	-5542.38	282.5	2204	S[1501]	-6226.18	282.5
2091	S[1388]	-4870.58	372.5	2148	S[1445]	-5554.38	372.5	2205	S[1502]	-6238.18	372.5
2092	S[1389]	-4882.58	192.5	2149	S[1446]	-5566.38	192.5	2206	S[1503]	-6250.18	192.5
2093	S[1390]	-4894.57	282.5	2150	S[1447]	-5578.37	282.5	2207	S[1504]	-6262.17	282.5
2094	S[1391]	-4906.57	372.5	2151	S[1448]	-5590.37	372.5	2208	S[1505]	-6274.17	372.5
2095	S[1392]	-4918.56	192.5	2152	S[1449]	-5602.36	192.5	2209	S[1506]	-6286.17	192.5
2096	S[1393]	-4930.56	282.5	2153	S[1450]	-5614.36	282.5	2210	S[1507]	-6298.16	282.5
2097	S[1394]	-4942.56	372.5	2154	S[1451]	-5626.36	372.5	2211	S[1508]	-6310.16	372.5
2098	S[1395]	-4954.55	192.5	2155	S[1452]	-5638.35	192.5	2212	S[1509]	-6322.15	192.5
2099	S[1396]	-4966.55	282.5	2156	S[1453]	-5650.35	282.5	2213	S[1510]	-6334.15	282.5
2100	S[1397]	-4978.55	372.5	2157	S[1454]	-5662.35	372.5	2214	S[1511]	-6346.15	372.5
2101	S[1398]	-4990.54	192.5	2158	S[1455]	-5674.34	192.5	2215	S[1512]	-6358.14	192.5
2102	S[1399]	-5002.54	282.5	2159	S[1456]	-5686.34	282.5	2216	S[1513]	-6370.14	282.5
2103	S[1400]	-5014.54	372.5	2160	S[1457]	-5698.34	372.5	2217	S[1514]	-6382.14	372.5
2104	S[1401]	-5026.53	192.5	2161	S[1458]	-5710.33	192.5	2218	S[1515]	-6394.13	192.5
2105	S[1402]	-5038.53	282.5	2162	S[1459]	-5722.33	282.5	2219	S[1516]	-6406.13	282.5
2106	S[1403]	-5050.53	372.5	2163	S[1460]	-5734.33	372.5	2220	S[1517]	-6418.13	372.5
2107	S[1404]	-5062.52	192.5	2164	S[1461]	-5746.32	192.5	2221	S[1518]	-6430.12	192.5
2108	S[1405]	-5074.52	282.5	2165	S[1462]	-5758.32	282.5	2222	S[1519]	-6442.12	282.5
2109	S[1406]	-5086.52	372.5	2166	S[1463]	-5770.32	372.5	2223	S[1520]	-6454.12	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2224	S[1521]	-6466.11	192.5	2281	S[1560]	-7149.91	192.5	2338	S[1617]	-7833.71	192.5
2225	S[1522]	-6478.11	282.5	2282	S[1561]	-7161.91	282.5	2339	S[1618]	-7845.71	282.5
2226	S[1523]	-6490.11	372.5	2283	S[1562]	-7173.91	372.5	2340	S[1619]	-7857.71	372.5
2227	S[1524]	-6502.10	192.5	2284	S[1563]	-7185.90	192.5	2341	S[1620]	-7869.70	192.5
2228	S[1525]	-6514.10	282.5	2285	S[1564]	-7197.90	282.5	2342	S[1621]	-7881.70	282.5
2229	S[1526]	-6526.10	372.5	2286	S[1565]	-7209.90	372.5	2343	S[1622]	-7893.70	372.5
2230	S[1527]	-6538.09	192.5	2287	S[1566]	-7221.89	192.5	2344	S[1623]	-7905.69	192.5
2231	S[1528]	-6550.09	282.5	2288	S[1567]	-7233.89	282.5	2345	S[1624]	-7917.69	282.5
2232	S[1529]	-6562.08	372.5	2289	S[1568]	-7245.89	372.5	2346	S[1625]	-7929.69	372.5
2233	S[1530]	-6574.08	192.5	2290	S[1569]	-7257.88	192.5	2347	S[1626]	-7941.68	192.5
2234	S[1531]	-6586.08	282.5	2291	S[1570]	-7269.88	282.5	2348	S[1627]	-7953.68	282.5
2235	S[1532]	-6598.07	372.5	2292	S[1571]	-7281.87	372.5	2349	S[1628]	-7965.68	372.5
2236	S[1533]	-6610.07	192.5	2293	S[1572]	-7293.87	192.5	2350	S[1629]	-7977.67	192.5
2237	S[1534]	-6622.07	282.5	2294	S[1573]	-7305.87	282.5	2351	S[1630]	-7989.67	282.5
2238	S[1535]	-6634.06	372.5	2295	S[1574]	-7317.86	372.5	2352	S[1631]	-8001.66	372.5
2239	S[1536]	-6646.06	192.5	2296	S[1575]	-7329.86	192.5	2353	S[1632]	-8013.66	192.5
2240	S[1537]	-6658.06	282.5	2297	S[1576]	-7341.86	282.5	2354	S[1633]	-8025.66	282.5
2241	S[1538]	-6670.05	372.5	2298	S[1577]	-7353.85	372.5	2355	S[1634]	-8037.65	372.5
2242	DUMMY[97]	-6682.05	192.5	2299	S[1578]	-7365.85	192.5	2356	S[1635]	-8049.65	192.5
2243	DUMMY[98]	-6694.05	282.5	2300	S[1579]	-7377.85	282.5	2357	S[1636]	-8061.65	282.5
2244	DUMMY[99]	-6706.04	372.5	2301	S[1580]	-7389.84	372.5	2358	S[1637]	-8073.64	372.5
2245	DUMMY[100]	-6718.04	192.5	2302	S[1581]	-7401.84	192.5	2359	S[1638]	-8085.64	192.5
2246	DUMMY[101]	-6730.04	282.5	2303	S[1582]	-7413.84	282.5	2360	S[1639]	-8097.64	282.5
2247	DUMMY[102]	-6742.03	372.5	2304	S[1583]	-7425.83	372.5	2361	S[1640]	-8109.63	372.5
2248	DUMMY[103]	-6754.03	192.5	2305	S[1584]	-7437.83	192.5	2362	S[1641]	-8121.63	192.5
2249	DUMMY[104]	-6766.03	282.5	2306	S[1585]	-7449.83	282.5	2363	S[1642]	-8133.63	282.5
2250	DUMMY[105]	-6778.02	372.5	2307	S[1586]	-7461.82	372.5	2364	S[1643]	-8145.62	372.5
2251	DUMMY[106]	-6790.02	192.5	2308	S[1587]	-7473.82	192.5	2365	S[1644]	-8157.62	192.5
2252	DUMMY[107]	-6802.01	282.5	2309	S[1588]	-7485.82	282.5	2366	S[1645]	-8169.62	282.5
2253	DUMMY[108]	-6814.01	372.5	2310	S[1589]	-7497.81	372.5	2367	S[1646]	-8181.61	372.5
2254	DUMMY[109]	-6826.01	192.5	2311	S[1590]	-7509.81	192.5	2368	S[1647]	-8193.61	192.5
2255	DUMMY[110]	-6838.00	282.5	2312	S[1591]	-7521.80	282.5	2369	S[1648]	-8205.61	282.5
2256	DUMMY[111]	-6850.00	372.5	2313	S[1592]	-7533.80	372.5	2370	S[1649]	-8217.60	372.5
2257	DUMMY[112]	-6862.00	192.5	2314	S[1593]	-7545.80	192.5	2371	S[1650]	-8229.60	192.5
2258	DUMMY[113]	-6873.99	282.5	2315	S[1594]	-7557.79	282.5	2372	S[1651]	-8241.59	282.5
2259	DUMMY[114]	-6885.99	372.5	2316	S[1595]	-7569.79	372.5	2373	S[1652]	-8253.59	372.5
2260	S[1539]	-6897.99	192.5	2317	S[1596]	-7581.79	192.5	2374	S[1653]	-8265.59	192.5
2261	S[1540]	-6909.98	282.5	2318	S[1597]	-7593.78	282.5	2375	S[1654]	-8277.58	282.5
2262	S[1541]	-6921.98	372.5	2319	S[1598]	-7605.78	372.5	2376	S[1655]	-8289.58	372.5
2263	S[1542]	-6933.98	192.5	2320	S[1599]	-7617.78	192.5	2377	S[1656]	-8301.58	192.5
2264	S[1543]	-6945.97	282.5	2321	S[1600]	-7629.77	282.5	2378	S[1657]	-8313.57	282.5
2265	S[1544]	-6957.97	372.5	2322	S[1601]	-7641.77	372.5	2379	S[1658]	-8325.57	372.5
2266	S[1545]	-6969.97	192.5	2323	S[1602]	-7653.77	192.5	2380	S[1659]	-8337.57	192.5
2267	S[1546]	-6981.96	282.5	2324	S[1603]	-7665.76	282.5	2381	S[1660]	-8349.56	282.5
2268	S[1547]	-6993.96	372.5	2325	S[1604]	-7677.76	372.5	2382	S[1661]	-8361.56	372.5
2269	S[1548]	-7005.96	192.5	2326	S[1605]	-7689.76	192.5	2383	S[1662]	-8373.56	192.5
2270	S[1549]	-7017.95	282.5	2327	S[1606]	-7701.75	282.5	2384	S[1663]	-8385.55	282.5
2271	S[1550]	-7029.95	372.5	2328	S[1607]	-7713.75	372.5	2385	S[1664]	-8397.55	372.5
2272	S[1551]	-7041.94	192.5	2329	S[1608]	-7725.75	192.5	2386	S[1665]	-8409.55	192.5
2273	S[1552]	-7053.94	282.5	2330	S[1609]	-7737.74	282.5	2387	S[1666]	-8421.54	282.5
2274	S[1553]	-7065.94	372.5	2331	S[1610]	-7749.74	372.5	2388	S[1667]	-8433.54	372.5
2275	S[1554]	-7077.93	192.5	2332	S[1611]	-7761.73	192.5	2389	S[1668]	-8445.54	192.5
2276	S[1555]	-7089.93	282.5	2333	S[1612]	-7773.73	282.5	2390	S[1669]	-8457.53	282.5
2277	S[1556]	-7101.93	372.5	2334	S[1613]	-7785.73	372.5	2391	S[1670]	-8469.53	372.5
2278	S[1557]	-7113.92	192.5	2335	S[1614]	-7797.72	192.5	2392	S[1671]	-8481.52	192.5
2279	S[1558]	-7125.92	282.5	2336	S[1615]	-7809.72	282.5	2393	S[1672]	-8493.52	282.5
2280	S[1559]	-7137.92	372.5	2337	S[1616]	-7821.72	372.5	2394	S[1673]	-8505.52	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2395	S[1674]	-8517.51	192.5	2452	S[1731]	-9201.31	192.5	2509	S[1788]	-9885.12	192.5
2396	S[1675]	-8529.51	282.5	2453	S[1732]	-9213.31	282.5	2510	S[1789]	-9897.11	282.5
2397	S[1676]	-8541.51	372.5	2454	S[1733]	-9225.31	372.5	2511	S[1790]	-9909.11	372.5
2398	S[1677]	-8553.50	192.5	2455	S[1734]	-9237.30	192.5	2512	S[1791]	-9921.10	192.5
2399	S[1678]	-8565.50	282.5	2456	S[1735]	-9249.30	282.5	2513	S[1792]	-9933.10	282.5
2400	S[1679]	-8577.50	372.5	2457	S[1736]	-9261.30	372.5	2514	S[1793]	-9945.10	372.5
2401	S[1680]	-8589.49	192.5	2458	S[1737]	-9273.29	192.5	2515	S[1794]	-9957.09	192.5
2402	S[1681]	-8601.49	282.5	2459	S[1738]	-9285.29	282.5	2516	S[1795]	-9969.09	282.5
2403	S[1682]	-8613.49	372.5	2460	S[1739]	-9297.29	372.5	2517	S[1796]	-9981.09	372.5
2404	S[1683]	-8625.48	192.5	2461	S[1740]	-9309.28	192.5	2518	S[1797]	-9993.08	192.5
2405	S[1684]	-8637.48	282.5	2462	S[1741]	-9321.28	282.5	2519	S[1798]	-10005.08	282.5
2406	S[1685]	-8649.48	372.5	2463	S[1742]	-9333.28	372.5	2520	S[1799]	-10017.08	372.5
2407	S[1686]	-8661.47	192.5	2464	S[1743]	-9345.27	192.5	2521	S[1800]	-10029.07	192.5
2408	S[1687]	-8673.47	282.5	2465	S[1744]	-9357.27	282.5	2522	S[1801]	-10041.07	282.5
2409	S[1688]	-8685.47	372.5	2466	S[1745]	-9369.27	372.5	2523	S[1802]	-10053.07	372.5
2410	S[1689]	-8697.46	192.5	2467	S[1746]	-9381.26	192.5	2524	S[1803]	-10065.06	192.5
2411	S[1690]	-8709.46	282.5	2468	S[1747]	-9393.26	282.5	2525	S[1804]	-10077.06	282.5
2412	S[1691]	-8721.45	372.5	2469	S[1748]	-9405.26	372.5	2526	S[1805]	-10089.06	372.5
2413	S[1692]	-8733.45	192.5	2470	S[1749]	-9417.25	192.5	2527	S[1806]	-10101.05	192.5
2414	S[1693]	-8745.45	282.5	2471	S[1750]	-9429.25	282.5	2528	S[1807]	-10113.05	282.5
2415	S[1694]	-8757.44	372.5	2472	S[1751]	-9441.24	372.5	2529	S[1808]	-10125.05	372.5
2416	S[1695]	-8769.44	192.5	2473	S[1752]	-9453.24	192.5	2530	S[1809]	-10137.04	192.5
2417	S[1696]	-8781.44	282.5	2474	S[1753]	-9465.24	282.5	2531	S[1810]	-10149.04	282.5
2418	S[1697]	-8793.43	372.5	2475	S[1754]	-9477.23	372.5	2532	S[1811]	-10161.03	372.5
2419	S[1698]	-8805.43	192.5	2476	S[1755]	-9489.23	192.5	2533	S[1812]	-10173.03	192.5
2420	S[1699]	-8817.43	282.5	2477	S[1756]	-9501.23	282.5	2534	S[1813]	-10185.03	282.5
2421	S[1700]	-8829.42	372.5	2478	S[1757]	-9513.22	372.5	2535	S[1814]	-10197.02	372.5
2422	S[1701]	-8841.42	192.5	2479	S[1758]	-9525.22	192.5	2536	S[1815]	-10209.02	192.5
2423	S[1702]	-8853.42	282.5	2480	S[1759]	-9537.22	282.5	2537	S[1816]	-10221.02	282.5
2424	S[1703]	-8865.41	372.5	2481	S[1760]	-9549.21	372.5	2538	S[1817]	-10233.01	372.5
2425	S[1704]	-8877.41	192.5	2482	S[1761]	-9561.21	192.5	2539	S[1818]	-10245.01	192.5
2426	S[1705]	-8889.41	282.5	2483	S[1762]	-9573.21	282.5	2540	S[1819]	-10257.01	282.5
2427	S[1706]	-8901.40	372.5	2484	S[1763]	-9585.20	372.5	2541	S[1820]	-10269.00	372.5
2428	S[1707]	-8913.40	192.5	2485	S[1764]	-9597.20	192.5	2542	S[1821]	-10281.00	192.5
2429	S[1708]	-8925.40	282.5	2486	S[1765]	-9609.20	282.5	2543	S[1822]	-10293.00	282.5
2430	S[1709]	-8937.39	372.5	2487	S[1766]	-9621.19	372.5	2544	S[1823]	-10304.99	372.5
2431	S[1710]	-8949.39	192.5	2488	S[1767]	-9633.19	192.5	2545	S[1824]	-10316.99	192.5
2432	S[1711]	-8961.38	282.5	2489	S[1768]	-9645.19	282.5	2546	S[1825]	-10328.99	282.5
2433	S[1712]	-8973.38	372.5	2490	S[1769]	-9657.18	372.5	2547	S[1826]	-10340.98	372.5
2434	S[1713]	-8985.38	192.5	2491	S[1770]	-9669.18	192.5	2548	S[1827]	-10352.98	192.5
2435	S[1714]	-8997.37	282.5	2492	S[1771]	-9681.17	282.5	2549	S[1828]	-10364.98	282.5
2436	S[1715]	-9009.37	372.5	2493	S[1772]	-9693.17	372.5	2550	S[1829]	-10376.97	372.5
2437	S[1716]	-9021.37	192.5	2494	S[1773]	-9705.17	192.5	2551	S[1830]	-10388.97	192.5
2438	S[1717]	-9033.36	282.5	2495	S[1774]	-9717.16	282.5	2552	S[1831]	-10400.96	282.5
2439	S[1718]	-9045.36	372.5	2496	S[1775]	-9729.16	372.5	2553	S[1832]	-10412.96	372.5
2440	S[1719]	-9057.36	192.5	2497	S[1776]	-9741.16	192.5	2554	S[1833]	-10424.96	192.5
2441	S[1720]	-9069.35	282.5	2498	S[1777]	-9753.15	282.5	2555	S[1834]	-10436.95	282.5
2442	S[1721]	-9081.35	372.5	2499	S[1778]	-9765.15	372.5	2556	S[1835]	-10448.95	372.5
2443	S[1722]	-9093.35	192.5	2500	S[1779]	-9777.15	192.5	2557	S[1836]	-10460.95	192.5
2444	S[1723]	-9105.34	282.5	2501	S[1780]	-9789.14	282.5	2558	S[1837]	-10472.94	282.5
2445	S[1724]	-9117.34	372.5	2502	S[1781]	-9801.14	372.5	2559	S[1838]	-10484.94	372.5
2446	S[1725]	-9129.34	192.5	2503	S[1782]	-9813.14	192.5	2560	S[1839]	-10496.94	192.5
2447	S[1726]	-9141.33	282.5	2504	S[1783]	-9825.13	282.5	2561	S[1840]	-10508.93	282.5
2448	S[1727]	-9153.33	372.5	2505	S[1784]	-9837.13	372.5	2562	S[1841]	-10520.93	372.5
2449	S[1728]	-9165.33	192.5	2506	S[1785]	-9849.13	192.5	2563	S[1842]	-10532.93	192.5
2450	S[1729]	-9177.32	282.5	2507	S[1786]	-9861.12	282.5	2564	S[1843]	-10544.92	282.5
2451	S[1730]	-9189.32	372.5	2508	S[1787]	-9873.12	372.5	2565	S[1844]	-10556.92	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2566	S[1845]	-10568.92	192.5	2623	S[1902]	-11252.72	192.5	2680	S[1959]	-11936.52	192.5
2567	S[1846]	-10580.91	282.5	2624	S[1903]	-11264.71	282.5	2681	S[1960]	-11948.51	282.5
2568	S[1847]	-10592.91	372.5	2625	S[1904]	-11276.71	372.5	2682	S[1961]	-11960.51	372.5
2569	S[1848]	-10604.91	192.5	2626	S[1905]	-11288.71	192.5	2683	S[1962]	-11972.51	192.5
2570	S[1849]	-10616.90	282.5	2627	S[1906]	-11300.70	282.5	2684	S[1963]	-11984.50	282.5
2571	S[1850]	-10628.90	372.5	2628	S[1907]	-11312.70	372.5	2685	S[1964]	-11996.50	372.5
2572	S[1851]	-10640.89	192.5	2629	S[1908]	-11324.69	192.5	2686	S[1965]	-12008.50	192.5
2573	S[1852]	-10652.89	282.5	2630	S[1909]	-11336.69	282.5	2687	S[1966]	-12020.49	282.5
2574	S[1853]	-10664.89	372.5	2631	S[1910]	-11348.69	372.5	2688	S[1967]	-12032.49	372.5
2575	S[1854]	-10676.88	192.5	2632	S[1911]	-11360.68	192.5	2689	S[1968]	-12044.48	192.5
2576	S[1855]	-10688.88	282.5	2633	S[1912]	-11372.68	282.5	2690	S[1969]	-12056.48	282.5
2577	S[1856]	-10700.88	372.5	2634	S[1913]	-11384.68	372.5	2691	S[1970]	-12068.48	372.5
2578	S[1857]	-10712.87	192.5	2635	S[1914]	-11396.67	192.5	2692	S[1971]	-12080.47	192.5
2579	S[1858]	-10724.87	282.5	2636	S[1915]	-11408.67	282.5	2693	S[1972]	-12092.47	282.5
2580	S[1859]	-10736.87	372.5	2637	S[1916]	-11420.67	372.5	2694	S[1973]	-12104.47	372.5
2581	S[1860]	-10748.86	192.5	2638	S[1917]	-11432.66	192.5	2695	S[1974]	-12116.46	192.5
2582	S[1861]	-10760.86	282.5	2639	S[1918]	-11444.66	282.5	2696	S[1975]	-12128.46	282.5
2583	S[1862]	-10772.86	372.5	2640	S[1919]	-11456.66	372.5	2697	S[1976]	-12140.46	372.5
2584	S[1863]	-10784.85	192.5	2641	S[1920]	-11468.65	192.5	2698	S[1977]	-12152.45	192.5
2585	S[1864]	-10796.85	282.5	2642	S[1921]	-11480.65	282.5	2699	S[1978]	-12164.45	282.5
2586	S[1865]	-10808.85	372.5	2643	S[1922]	-11492.65	372.5	2700	S[1979]	-12176.45	372.5
2587	S[1866]	-10820.84	192.5	2644	S[1923]	-11504.64	192.5	2701	S[1980]	-12188.44	192.5
2588	S[1867]	-10832.84	282.5	2645	S[1924]	-11516.64	282.5	2702	S[1981]	-12200.44	282.5
2589	S[1868]	-10844.84	372.5	2646	S[1925]	-11528.64	372.5	2703	S[1982]	-12212.44	372.5
2590	S[1869]	-10856.83	192.5	2647	S[1926]	-11540.63	192.5	2704	S[1983]	-12224.43	192.5
2591	S[1870]	-10868.83	282.5	2648	S[1927]	-11552.63	282.5	2705	S[1984]	-12236.43	282.5
2592	S[1871]	-10880.82	372.5	2649	S[1928]	-11564.62	372.5	2706	S[1985]	-12248.43	372.5
2593	S[1872]	-10892.82	192.5	2650	S[1929]	-11576.62	192.5	2707	S[1986]	-12260.42	192.5
2594	S[1873]	-10904.82	282.5	2651	S[1930]	-11588.62	282.5	2708	S[1987]	-12272.42	282.5
2595	S[1874]	-10916.81	372.5	2652	S[1931]	-11600.61	372.5	2709	S[1988]	-12284.41	372.5
2596	S[1875]	-10928.81	192.5	2653	S[1932]	-11612.61	192.5	2710	S[1989]	-12296.41	192.5
2597	S[1876]	-10940.81	282.5	2654	S[1933]	-11624.61	282.5	2711	S[1990]	-12308.41	282.5
2598	S[1877]	-10952.80	372.5	2655	S[1934]	-11636.60	372.5	2712	S[1991]	-12320.40	372.5
2599	S[1878]	-10964.80	192.5	2656	S[1935]	-11648.60	192.5	2713	S[1992]	-12332.40	192.5
2600	S[1879]	-10976.80	282.5	2657	S[1936]	-11660.60	282.5	2714	S[1993]	-12344.40	282.5
2601	S[1880]	-10988.79	372.5	2658	S[1937]	-11672.59	372.5	2715	S[1994]	-12356.39	372.5
2602	S[1881]	-11000.79	192.5	2659	S[1938]	-11684.59	192.5	2716	S[1995]	-12368.39	192.5
2603	S[1882]	-11012.79	282.5	2660	S[1939]	-11696.59	282.5	2717	S[1996]	-12380.39	282.5
2604	S[1883]	-11024.78	372.5	2661	S[1940]	-11708.58	372.5	2718	S[1997]	-12392.38	372.5
2605	S[1884]	-11036.78	192.5	2662	S[1941]	-11720.58	192.5	2719	S[1998]	-12404.38	192.5
2606	S[1885]	-11048.78	282.5	2663	S[1942]	-11732.58	282.5	2720	S[1999]	-12416.38	282.5
2607	S[1886]	-11060.77	372.5	2664	S[1943]	-11744.57	372.5	2721	S[2000]	-12428.37	372.5
2608	S[1887]	-11072.77	192.5	2665	S[1944]	-11756.57	192.5	2722	S[2001]	-12440.37	192.5
2609	S[1888]	-11084.76	282.5	2666	S[1945]	-11768.57	282.5	2723	S[2002]	-12452.37	282.5
2610	S[1889]	-11096.76	372.5	2667	S[1946]	-11780.56	372.5	2724	S[2003]	-12464.36	372.5
2611	S[1890]	-11108.76	192.5	2668	S[1947]	-11792.56	192.5	2725	S[2004]	-12476.36	192.5
2612	S[1891]	-11120.75	282.5	2669	S[1948]	-11804.55	282.5	2726	S[2005]	-12488.36	282.5
2613	S[1892]	-11132.75	372.5	2670	S[1949]	-11816.55	372.5	2727	S[2006]	-12500.35	372.5
2614	S[1893]	-11144.75	192.5	2671	S[1950]	-11828.55	192.5	2728	S[2007]	-12512.35	192.5
2615	S[1894]	-11156.74	282.5	2672	S[1951]	-11840.54	282.5	2729	S[2008]	-12524.34	282.5
2616	S[1895]	-11168.74	372.5	2673	S[1952]	-11852.54	372.5	2730	S[2009]	-12536.34	372.5
2617	S[1896]	-11180.74	192.5	2674	S[1953]	-11864.54	192.5	2731	S[2010]	-12548.34	192.5
2618	S[1897]	-11192.73	282.5	2675	S[1954]	-11876.53	282.5	2732	S[2011]	-12560.33	282.5
2619	S[1898]	-11204.73	372.5	2676	S[1955]	-11888.53	372.5	2733	S[2012]	-12572.33	372.5
2620	S[1899]	-11216.73	192.5	2677	S[1956]	-11900.53	192.5	2734	S[2013]	-12584.33	192.5
2621	S[1900]	-11228.72	282.5	2678	S[1957]	-11912.52	282.5	2735	S[2014]	-12596.32	282.5
2622	S[1901]	-11240.72	372.5	2679	S[1958]	-11924.52	372.5	2736	S[2015]	-12608.32	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2737	S[2016]	-12620.32	192.5	2794	PASS1_R	-13304.12	192.5				
2738	S[2017]	-12632.31	282.5	2795	PASS1_R	-13316.11	282.5				
2739	S[2018]	-12644.31	372.5	2796	PASS1_R	-13328.11	372.5				
2740	S[2019]	-12656.31	192.5	2797	DUMMY[121]	-13340.11	192.5				
2741	S[2020]	-12668.30	282.5	2798	DUMMY[122]	-13352.10	282.5				
2742	S[2021]	-12680.30	372.5	2799	DUMMY[123]	-13364.10	372.5				
2743	S[2022]	-12692.30	192.5	2800	DUMMY[124]	-13376.10	192.5				
2744	S[2023]	-12704.29	282.5	2801	DUMMY[125]	-13388.09	282.5				
2745	S[2024]	-12716.29	372.5	2802	DUMMY[126]	-13400.09	372.5				
2746	S[2025]	-12728.29	192.5	2803	DUMMY[127]	-13412.09	192.5				
2747	S[2026]	-12740.28	282.5	2804	DUMMY[128]	-13424.08	282.5				
2748	S[2027]	-12752.28	372.5	2805	DUMMY[129]	-13436.08	372.5				
2749	S[2028]	-12764.27	192.5								
2750	S[2029]	-12776.27	282.5								
2751	S[2030]	-12788.27	372.5								
2752	S[2031]	-12800.26	192.5								
2753	S[2032]	-12812.26	282.5								
2754	S[2033]	-12824.26	372.5								
2755	S[2034]	-12836.25	192.5								
2756	S[2035]	-12848.25	282.5								
2757	S[2036]	-12860.25	372.5								
2758	S[2037]	-12872.24	192.5								
2759	S[2038]	-12884.24	282.5								
2760	S[2039]	-12896.24	372.5								
2761	S[2040]	-12908.23	192.5								
2762	S[2041]	-12920.23	282.5								
2763	S[2042]	-12932.23	372.5								
2764	S[2043]	-12944.22	192.5								
2765	S[2044]	-12956.22	282.5								
2766	S[2045]	-12968.22	372.5								
2767	S[2046]	-12980.21	192.5								
2768	S[2047]	-12992.21	282.5								
2769	S[2048]	-13004.20	372.5								
2770	S[2049]	-13016.20	192.5								
2771	S[2050]	-13028.20	282.5								
2772	S[2051]	-13040.19	372.5								
2773	DUMMY[115]	-13052.19	192.5								
2774	DUMMY[116]	-13064.19	282.5								
2775	DUMMY[117]	-13076.18	372.5								
2776	DUMMY[118]	-13088.18	192.5								
2777	DUMMY[119]	-13100.18	282.5								
2778	DUMMY[120]	-13112.17	372.5								
2779	PASS2_R	-13124.17	192.5								
2780	PASS2_R	-13136.17	282.5								
2781	PASS2_R	-13148.16	372.5								
2782	PASS2_R	-13160.16	192.5								
2783	PASS2_R	-13172.16	282.5								
2784	PASS2_R	-13184.15	372.5								
2785	VCOM	-13196.15	192.5								
2786	VCOM	-13208.15	282.5								
2787	VCOM	-13220.14	372.5								
2788	VCOM	-13232.14	192.5								
2789	VCOM	-13244.13	282.5								
2790	VCOM	-13256.13	372.5								
2791	PASS1_R	-13268.13	192.5								
2792	PASS1_R	-13280.12	282.5								
2793	PASS1_R	-13292.12	372.5								

15. REVISION HISTORY

Revision	Content	Page	Date
0.1	New SPEC	-	2016/01/06